QUASI-RESONANT SOFT-SWITCHING INVERTERS FOR POWER SUPPLIES AND INDUCTION MOTOR DRIVES

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By

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CERTIFICATE

It is certified that the work contained in this thesis entitled "***Quasi-Resonant Soft-Switching Inverters for Power Supplies and Induction Motor Drives***" by **Sribatsa Behera,** has been carried out under our supervision and that work has not been submitted elsewhere for any degree.

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Dedicated
to the memory of

My

Beloved
Grandmother

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ABSTRACT

Soft-switched dc-ac inverters are attractive for power supply and motor drive applications due to distinct advantages such as high efficiency, high frequency operation, compact structure, and low EMI etc. compared to hard-switched converters. The present thesis deals with design, simulation and laboratory implementation of various quasi-resonant dc link inverters for different loads.

Initially, a novel quasi-resonant dc link (QRDCL) inverter comprising of two switches and three resonant components is proposed for high power factor loads. Simulation of the inverter under modified space vector modulation (MSVM) for an R-L load at 400 Hz is carried out. The MSVM is developed incorporating soft-switching technique. It differs from the conventional space vector modulation (SVM) in implementing zero vectors. The resonant components are designed and a laboratory-sized model is fabricated and tested. Test results agree with simulation results showing soft-switching of devices in the resonant link and the inverter.

The inverter proposed earlier has the limitation that it can operate only with high power factor loads. Another novel QRDCL inverter suitable for high as well as low power factor loads is proposed. The quasi-resonant link comprises of four switches and three resonant components. The inverter operates satisfactorily with positive and negative dc link current. The simulation is carried out with the help of SABER incorporating MSVM control technique. Experiment is conducted with both R-L and induction motor loads. Simulation and experimental results reveal soft-switching with low and high power factor loads.

A high performance induction motor drive is operated using QRDCL inverter incorporating direct torque control (DTC) scheme. The DTC scheme along with QRDCL inverter is analyzed by SABER Simulator. The soft-switching of inverter devices, independent control of torque and flux are verified from simulation. Further, the simulation is extended to include a reduced-order stator flux observer robust to speed variation. From the SABER simulation of the observer-based DTC scheme, it is found that the stator flux from the observer follows closely the flux obtained from the mathematical model of the induction machine. The experiment is conducted on a laboratory-sized induction machine for both with and without observer. The results obtained

from the experiment compare well with those obtained from simulation.

The detailed study of QRDCL inverter reveals that it can be used not only for power supplies but also to high performance induction motor drives. Because of soft-switching and high performance of the inverter, it can find application in airborne power supplies where size, and weight due to paucity of space are of paramount importance.

Key words: *Dc-ac converters (inverters), quasi-resonant dc link (QRDCL) inverter, High and low power factor loads, Modified space vector modulation, high performance induction motor drive, and robust reduced order stator flux observer.*

SYNOPSIS

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Dc to ac power conversion using pulse width modulation (PWM) within inverters has been widely known for more than three decades. Even today, PWM inverters play a major role in the area of power supplies and drives. However, these converters suffer from high switching losses and stresses, and produce electro-magnetic interference (EMI) when operated at high frequencies. As a result, the size, volume and weight of these converters increase due to high snubber ratings, large size of heat sinks and EMI filters. These shortcomings are minimized using the principle of zero-voltage switching (ZVS) and/or zero-current switching (ZCS) for the switching devices. The switching devices are turned on/off under zero-voltage and/or zero-current switchings created by the resonant circuit. The resonant circuit usually comprises various combinations of resonant inductors, capacitors, and sometimes switching devices. The ZVS and ZCS operation of power devices is popularly known as soft-switching. By replacing the dc link in a PWM inverter with a parallel resonant dc link, the familiar parallel resonant dc link (PRDCL) inverter is obtained. As a result, the performance of these converters improves

significantly. The major problem with the PRDCL inverter is that the link oscillates for the entire period of switching cycle during which the associated passive LC components carry the full-load current, and the switching devices are stressed to more than twice the source voltage. This necessitates the use of higher-rated resonant components and devices. Thus, the size and weight of resonant components increase and finally add to the net weight and volume of inverters. To overcome these problems, actively clamped parallel resonant dc link inverters (ACPRDCL) were proposed. In ACPRDCL inverters, the clamping voltage is maintained within a range of 1.3 to 1.8 times the source voltage. The problems of ACRDCL are partially eliminated using reduced voltage parallel resonant dc link inverters (RVPRDCL) in which the switching devices of the inverter are stressed within 1.2 to 1.4 times the source voltage. It is found that the above topologies (i.e., PRDCL, ACPRDCL, RVPRDCL) are not completely free from switching stresses. Besides, the resonant components in these topologies continue to carry the normal load current throughout the resonant period. These shortcomings are overcome by using quasi-resonant dc link (QRDCL) inverters. In quasi-resonant dc link (QRDCL) inverters, each switching cycle has two intervals. One is the resonant interval and the other is the non-resonant interval. The resonant interval constitutes a small interval of the switching cycle. During the resonant interval, the resonant network is activated to enable soft-switching of power devices in the dc link as well as in the inverter. This soft-switching is implemented using either zero-voltage transition (ZVT) or zero-current transition (ZCT). The circulating energy associated with soft-switching transition due to resonance is quite small. The resonant components are involved with the load current only during resonant interval and remain dormant during non-resonant interval. Further, the resonant dc link voltage is always clamped to the source voltage. Since the resonant components are involved during a small interval of the switching cycle, their VA ratings and size become quite small. As a result, the inverters become more efficient, lighter in weight, and compact. Because of several merits mentioned above, the quasi-resonant dc link inverters are preferred over resonant dc link inverters. In this thesis two novel topologies of quasi-resonant dc link inverters are proposed. Attempts have been made to successfully incorporate soft-switching in all devices in the inverter and the dc link as well. Such inverters are expected to find application in high frequency airborne ac power supplies and high performance induction motor drives.

Initially, a novel quasi-resonant dc link inverter is proposed for high power factor load. The topology comprises two switches, a resonant inductor and two resonant capacitors. Modified space vector modulation (MSVM) is used in order to implement soft-switching for all devices in the inverter and the resonant link. Zero vectors are implemented in the MSVM in a manner different from that in the conventional space vector modulation (SVM). The complete circuit is modeled and analyzed by SABER simulator. A proto-type laboratory-sized model of QRDCL three-phase inverter is built and the experiment is conducted at the output frequency of 400 Hz with balanced three-phase RL load. There is a good agreement between simulation and experimental results. Both simulation and experimental results show soft-switching for all devices. The total harmonic distortion (THD) and efficiency are also obtained.

In this topology, the dc link input current to the three-phase inverter is always found to be positive due to high power factor load. The topology cannot operate under soft-switching for low power factor load due to presence of negative dc link current. Hence, the quasi-resonant link needs to be modified if the three-phase inverter is to be operated under low power factor load. It is, therefore, desirable to have an inverter, which can work with low and high power factor load.

The circuit proposed earlier is modified and a novel quasi-resonant dc link inverter topology is proposed for low and high power factor load. The topology is capable of handling both high and low power factor load with soft-switching. The topology has two pairs of switches. One of these is in between the source and the dc link, and other is across the dc link. This QRDCL inverter topology provides soft-switching operation of inverter devices independent of direction of the dc link current. The complete system is modeled both for R-L and induction motor loads under MSVM. The performance of the system (such as losses and THD) with different resonant parameters is analyzed with SABER simulator. A laboratory-sized model is fabricated and experimentally tested to compare the simulation results for both R-L and induction motor loads. The waveform of the phase current is close to sinusoidal and there is good agreement between simulation and experimental results.

The total harmonic distortion (THD) has been shown to be in the range 6 to 8% through

simulation while the same by experiment has been found to be in range of 8 to 10%. The efficiency obtained by simulation has been in the range of 94 to 96% while the same by experiment has been found to be in the range of 90 to 91%.

After successful operation of the proposed topology with low and high power factor load, the soft-switching operation of this scheme is extended to a high performance direct torque controlled induction motor drive. In this, the QRDCL inverter replaces the conventional inverter of the drive. The d-q model of the complete scheme is formulated and analyzed by SABER simulator. The experiment is conducted on a laboratory-sized induction motor. The results from both simulation and experiment reveal soft-switching of devices in the inverter and dc link. Responses of speed and stator flux from the simulation agree with those from experiment during step change in the reference speed command and the four-quadrant operation. It is also observed that the stator flux response remains unchanged during reversal of speed. The stator d- and q-axis fluxes from simulation agree with those from experiment. The scheme is further extended to include a robust, reduced order stator flux observer. The observer gain is properly designed and tuned to work satisfactorily with the experimental setup. The reduced-order stator flux observer is then implemented and tested on the same laboratory-sized model without any additional hardware except small changes in program. The results obtained from the schemes with the observer and without the observer have been compared. They are found to be in good agreement.

In conclusion, two novel soft-switching quasi-resonant dc link inverter topologies have been studied. Initially a topology is developed to handle only high power factor load. This limitation is overcome by another novel topology, which successfully handles both low and high power factor loads. Both topologies have been investigated in detail. The inverters are controlled using modified state vector modulation (MSVM). The proposed quasi-resonant dc link topologies always limit the peak resonant voltage to the source voltage. This feature, coupled with the soft-switching of all devices, makes the complete inverter system economical and efficient due to reduced size, weight and switching losses. The results of simulation study of QRDCL inverters by SABER software have been validated by the experimental results on a laboratory-sized model. The THD of the output phase current is found to decrease significantly with an increase

in the switching frequency. After the successful implementation of QRDCL inverter for high and low power factor load, the operation is extended to the direct torque controlled induction motor drive. The ZVS operation for all switching devices in the inverter has been achieved. This drive scheme is also studied with a robust reduced order stator flux observer. It is seen that the use of reduced order observer has made it possible to accurately track the machine-model flux with improved dynamics.

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List of Symbols

C_r, C_{r1}, C_{r2}, C_h	Resonant capacitors
C_c	Clamping capacitor
C_{snub}	Snubber capacitor
C_d	Biasing capacitor
D_{ap}, D_{bp}, D_{cp}, D_{an}, D_{bn}, D_{cn}	Feedback diodes across three phase inverter switches
D_{fb}, D_p , $D_{1\text{-}SH}$, $D_{2\text{-}SH}$	Feedback diodes in resonant circuit
D_1, D_2	Diodes in resonant network.
D_f	Free-wheeling diode
f_{sw}	Switching frequency
G_A, G_M	Gate pulses to auxiliary switch SW_A and main switch SW_M
G_{SH}	Gate pulse to shunt switches $SW_{1\text{-}SH}$ and $SW_{2\text{-}SH}$
G_1 .. G_6	Gate pulses of inverter switches
i_a, i_b, i_c	Three phase currents of inverter
i_{Link}	Input dc link current to the three-phase inverter
i_{swa}, i_{swm}	Currents through switches SW_A and SW_M respectively
i_{Lr}, i_{Lsh}	Currents through resonant inductors, L_r and L_{sh} respectively
i_{Cr1}, i_{Cr2}	Currents through capacitors Cr_1 and Cr_2 respectively
i_{Df}, i_{Dp}	Currents through diodes D_f and D_p
i_{qs}, i_{ds}	The stator d-axis and q-axis currents
L_r, L_{sh}, L_A, L_B, L_C	Resonant inductors
L_d	Biasing inductor
L_s, L_r	Per-phase total stator and rotor inductances of induction motor
L_m	Per-phase magnetizing inductance of induction motor
N_{ref}	Reference speed command
N_{act}	Actual rotor speed
S_{ap}, S_{bp}, S_{cp}	Upper half switches of three-phase inverter
S_{an}, S_{bn}, S_{cn}	Lower half switches of three-phase inverter

SW_A	Auxiliary switch in resonant tank
SW_M	Main switch in resonant tank
$SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$	Shunt switches in resonant tank
S, S_r	Switches in resonant tank
S_a, S_b, S_c	Switching status of inverter switches
t_{aux}	Duration of pulse of switch SW_A in resonant network
t_{main}	Duration of pulse of switch SW_M in resonant network
t_{sect}	Duration of sector
r_s	Per-phase stator resistance of induction motor
r_r	Per-phase stator equivalent rotor resistance of induction motor
T_{ref}	Reference torque
T_{act}	Actual torque developed by induction motor
T_L	Load torque
T_s	Switching period
T_{st}	Torque status
S_1.. S_6	Six sectors
t_1, t_2	Duration of nonzero voltage vectors
t_{z1}, t_{z2}	Duration of two zero vectors
V_1..V_6	Non-zero voltage vectors
V_0, V_7, V_{z1}, V_{z2}	Zero voltage vectors
V_{ds}, V_{qs}	Stator d- and q-axes voltages
V_{Cr}	Dc link capacitor voltage
V_{swa}, V_{swm}	Voltage across SW_A and SW_M
V_{dc}	Input dc voltage to the inverter
Varm	Armature voltage of dc generator coupled with induction motor
w_r	Angular electrical speed of rotor of induction motor
Ψ_{ds}, Ψ_{qs}	Stator d- and q-axes fluxes of induction motor
Ψ_s	Stator flux of induction motor
Ψ_{st}	Flux status

$\Psi_{s\text{-}obs}$	Stator flux obtained from observer
$\Psi_{s\text{-}mod}$	Stator flux obtained from induction motor model
$\Delta\Psi_s$, ΔT	Flux band and torque band
σ	Leakage factor

(All induction motor parameters are referred to the primary side. Boldface letter/ sym represents matrix or vector.)

CHAPTER 1

Introduction

1.1 The PWM Inverter

Dc to ac power conversion using Pulse Width Modulation (PWM) within inverters has bee widely known for the last three decades. The attractiveness of the PWM inverter is that it has simple power structure and possesses six self-commutating devices. The anti-parallel diod required are typically mounted in the same device package for minimum lead inductance ar ease of assembly. The control strategy is reasonably simple and provides a fully regenerati interface between the dc source and ac load. These inverters find applications in uninterruptib power supplies, motor drives, induction heating etc. In spite of the above merits, the PW inverter suffers from the following limitations:

- Low switching frequencies due to high switching losses.
- Power devices are subjected to high switching stresses (peak current and voltag during turn-on and turn-off transients. This requires large safe-operating area (SO specifications for the devices.
- Acoustic noise at inverter switching frequency is unacceptable.
- Dc link and ac side filters are too large.
- Severe di/dt and dv/dt produce electromagnetic interference (EMI).
- Low power density.
- Increased size and weight.

2 The Resonant DC Link (RDCL) Inverter

To eliminate these shortcomings, the principle of zero-voltage switching (ZVS) or zero-rrent switching (ZCS) is applied. It means the switching devices of the inverter are turned /off under either zero-voltage or zero-current condition. ZVS and ZCS are referred to as soft-vitching techniques in the technical literature. The resonant circuit, which creates ZVS and CS conditions for switching devices, comprises various combinations of passive components ich as resonant inductors and capacitors. The resonant circuits also possess active switches, ferred to as resonant switches, which along with resonant LC components produce resonance) as to realize soft-switching of inverter devices. These resonant circuits can be accommodated ther at the input or the output of the inverters depending upon circumstances. In the resonant nk inverters, the link is made to oscillate at a high frequency. All the devices that are connected) the link are turned on or off using either ZVS or ZCS technique so that the switching losses re greatly reduced. Fig. 1.1 shows the device switching loci for hard-switching and soft-witching. The switching losses in a device are proportional to the area under the curve.

Comparison of hard- and soft-switching areas reveals that there is a significant reduction in osses in soft-switching. This permits operation of an inverter at high frequencies without any ignificant increase in switching losses. Soft-switching also eliminates many other problems ncountered in hard-switching, as mentioned in 1.1. Hence the performance of the inverter can e greatly improved by the use of soft-switched resonant link inverter. In resonant link inverters, he link periodically generates either alternating or unidirectional signals of voltages or currents cross the input of the inverter. Thus depending upon the configuration, the resonant link can be he resonant ac link (RACL) or the resonant dc link (RDCL). The earliest and the most mature soft-switching inverter topology is the RDCL inverter, which requires fewer devices as compared to the RACL. In the case of the resonant dc link (RDCL) inverters [12-17], the resonant network is placed between the dc source and the inverter. The link periodically generates varying unidirectional voltage or current pulses across the input of the inverter. RDCL with varying unidirectional voltage pulses is more economical than same with varying current pulses. This RDCL circuit is enabled for ZVS when a change in the switching status of the

inverter is desired. Attempts to improve upon the basic RDCL inverter have been made by various researchers. Parallel RDCL (PRDCL) [16-17], actively clamped PRDCL (ACPRDCL) [19-22] and reduced voltage PRDCL (RVPRDCL) inverter [23] topologies have appeared in the literature. The underlying principle in all these versions has remained the same as that in RDCL.

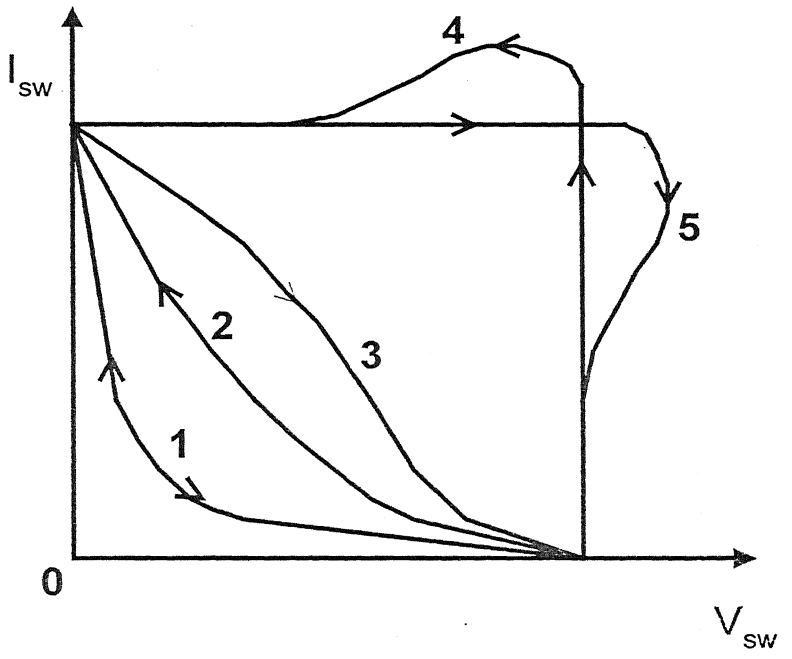


Fig. 1.1 Switching Loci
1: Turn on/off at ZVS/ZCS (*Soft-switchings*)
2: Turn-on with snubber, **3**: Turn-off with snubber
4: Turn-on without snubber, **5**: Turn-off without snubber
(4 & 5: *Hard-switching*)
Isw :- Current through the switch
Vsw:- Voltage across the switch

1.3 The Quasi-Resonant DC Link (QRDCL) Inverter

The major problem with RDCL inverters is that the link continuously oscillates for the ent period of the switching cycle. During this period the associated resonant components carry

full-load current. This necessitates the use of higher-rated resonant components. Thus, the size, volume, and weight of the resonant components increase, adding to the net weight and volume of the inverters. The problems of RDCL are overcome using the quasi-resonant dc link (QRDCL) inverters. In QRDCL inverters [33, 34-36, 40-44], the resonant mode of operation occurs during a small part of the switching cycle, only when an inverter device needs to be turned on or off. Hence the resonant components do not carry the normal load current during the entire switching cycle. Since the resonant components are active only during a small interval of the switching cycle, the size and volume of the resonant components are significantly reduced. This leads to inverters of a compact size and weight.

1.4 Organization of the Thesis

The thesis is organized into six chapters.

Chapter 1 discusses the principle of soft-switching and the objectives of the quasi-resonant dc link inverter.

Chapter 2 presents a review of different types of resonant links. The categorization of resonant links is presented along with a discussion of the advantages and disadvantages of the individual schemes. It is followed by a brief survey of the modifications suggested by various authors. Various control strategies used in inverters such as conventional PWM techniques and space vector modulation (SVM) technique are discussed.

Chapter 3 deals with the design, development and implementation of a novel quasi-resonant dc link (QRDCL) inverter for high power factor load. A two-switch topology is proposed for this inverter. As for the control strategy, a modified space vector modulation technique (MSVM) for soft-switching of the three phase quasi-resonant dc link inverter is presented and analyzed by SABER simulator. A proto-type laboratory-sized model of the proposed QRDCL inverter is built and the experiment is conducted with a balanced RL load for the three-phase inverter. The performance of this system is compared with the results obtained from simulation and from an

experimental setup under identical operating conditions. In this case, the dc link input current to the three-phase inverter is always positive (i.e., from source to inverter). This topology cannot operate under soft-switching for low power factor load due to the presence of the negative dc link current (i.e., from inverter to source / regenerative condition).

Chapter 4 deals with the design, development and implementation of a novel QRDCL inverter for both low and high power factor load. The proposed topology consists of four switches (i.e., two switches in series and other two across the dc link). The soft-switching operation of the inverter devices is independent of the direction of the dc link current. This topology is modeled both for the R-L load and a three-phase induction motor load under MSVM control. The performance of this topology (such as losses and THD) at varying parameters is analyzed with SABER simulator and presented in the form of tables. A laboratory-sized model is fabricated and experimentally tested to compare the simulation results under identical operating conditions for both static and active loads (induction motor load).

Chapter 5 extends the soft-switching technique of the topology of Chapter 4 to a high performance induction motor drive. In this case, the quasi-resonant dc link (QRDCL) inverter replaces the conventional inverter of the drive system. A new control strategy other than MSVM is evolved to operate the inverter devices under soft-switching conditions. The d-q model of the complete scheme is formulated and analyzed by SABER simulator. The experiment is conducted on a proto-type induction motor. Comparative results of simulation and experiments under identical operating conditions are presented. The simulation is extended to include a robust, reduced order stator flux-based observer. The scheme with the observer is implemented on a laboratory-sized experimental set-up, and the performance of the drive system with and without the observer is compared.

Chapter 6 concludes the thesis with suggestions for further research work.

CHAPTER 2

Soft-Switching Converters – A Literature Review

2.1 Introduction

In conventional dc-ac power conversion, the input to three-phase PWM inverters is a stiff dc voltage supply and the power switches operate in a switch mode. Therefore, the power devices are subjected to high switching stresses and switching power losses that increase linearly with the switching frequency of pulse-width modulation. High switching power losses not only restrict switching frequency, but also reduce the system efficiency and produce tremendous heat inside the inverter. This compels the industrial personnel to use larger heat sinks, which result in increased volume and weight of the system. In addition to these limitations, the system suffers from other shortcomings such as EMI and acoustic noise.

The increased demand for high power density converters in aerospace, defence and telecommunications has prompted researchers to design converters capable of operating at a high switching frequency and without adverse effects of PWM converters. These application areas also impose constraints upon the size, weight and volume of converters to enable them to accommodate greater payloads. The benefits of high frequency converters have been recognized and their importance has significantly increased. Remarkable efforts have been made in the development of high-frequency zero-voltage switching (ZVS) and zero-current switching (ZCS) dc-ac power converters, which can now realize power supplies that are highly dynamic, high performance with negligible noise. In these converters, the principle of resonance is used in order to implement the soft-switching techniques (ZVS/ZCS) for various devices in the resonant link and the inverter. These resonant links are embedded in different locations of the inverters depending upon their configuration. The progress of soft-switching techniques has passed through various stages during the last two decades. In this chapter, a literature review of the various types of resonant link inverters is undertaken. For each type, its merits and limitations are pointed out. An in-depth study is undertaken in the case of quasi-

resonant dc link inverter. Modifications suggested by many authors in QRDCL topology are presented. The various types of resonant dc-ac converters are shown in Fig. 2.1. The classification of resonant links is based on the location of the resonant network with respect to load, inverter and dc bus in the converter systems, characteristics of switch waveforms (ZVS/ZCS), and types of resonance (series/parallel).

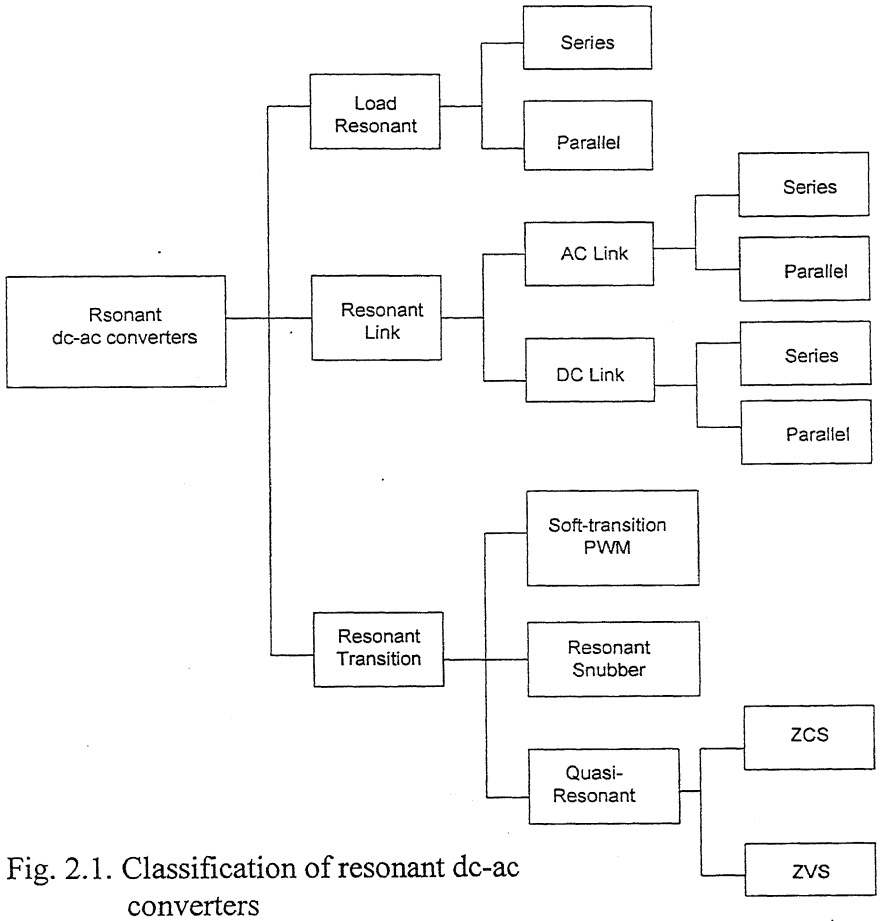
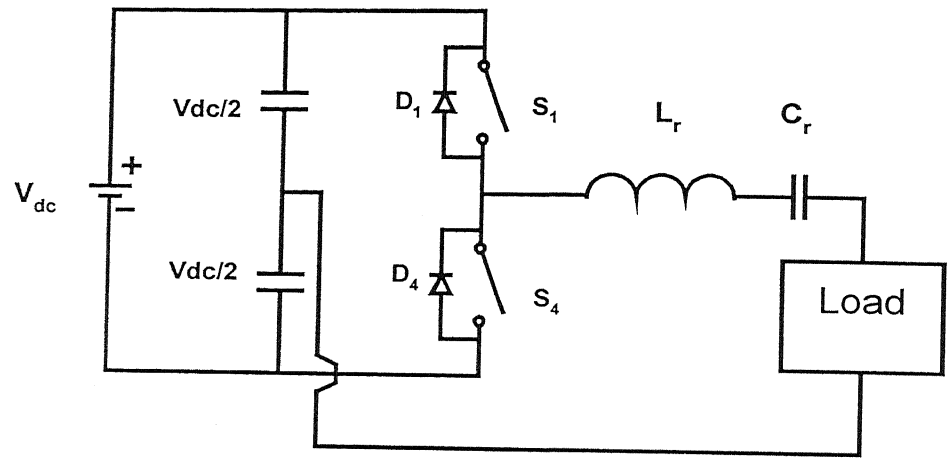


Fig. 2.1. Classification of resonant dc-ac converters

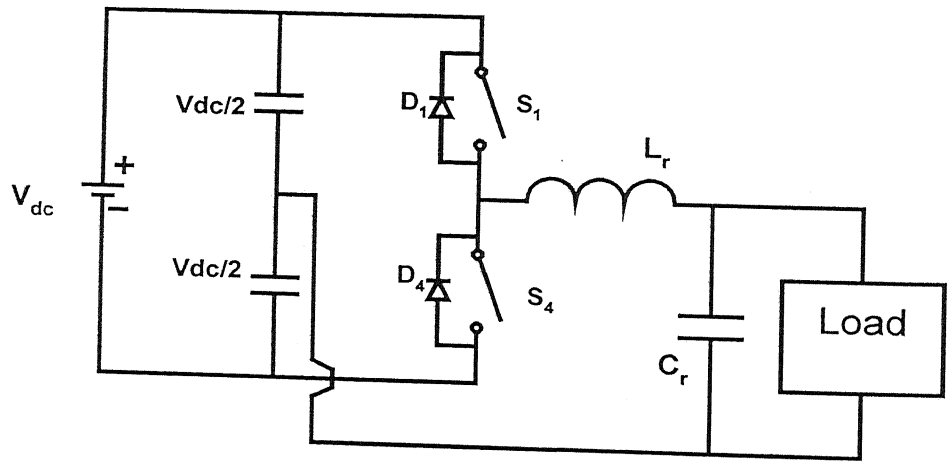
2.2 Load Resonant DC-AC Converters

Various topologies of load resonant dc-ac converters have been reported [1-6]. Jain et al. [1] proposed a topology for aerospace application. The authors in [2] proposed a thyristor-based topology for welding purposes. Batarseh [7] presented different combinations of LC components for these dc-ac converters. A generalized program for extracting control

characteristics via the state-plane diagram is reported in [8]. The load resonant dc-ac converters are classified into series-loaded resonant (SLR) and parallel-loaded resonant (PLR) types. Typical cases of series and parallel resonant half-bridge dc-ac converters are shown in Fig. 2.2.



(a)



(b)

Fig. 2.2. Load resonant dc-ac converter
(a) Series-loaded resonant dc-ac converter
(b) Parallel-loaded resonant dc-ac converter

In load resonant dc-ac converters, an LC resonant tank is added to the load side in series, in parallel, or in a combination of series and parallel LC schemes. The resonant tank oscillates with a resonant frequency (f_r) during the entire switching period ($T_s = 1/f_s$, f_s is converter frequency). As a result, the resonant tank produces the oscillating load voltage and current waveforms, which create ZVS and/or ZCS conditions for the switching devices. In either case (i.e., SLR or PLR), the resonant period decides the conduction of switching devices. The nature of the current in the output is controlled by the relationship between f_s and f_r (i.e., $f_s < f_r/2$, $f_r/2 < f_s < f_r$, $f_s > f_r$). For $f_s < f_r/2$, the load current is discontinuous and this becomes continuous for $f_s > f_r/2$. In case of SLR, it is possible to use thyristors as switches at a low switching frequency (i.e., $f_s < f_r$), whereas the self-commutated switches are used for $f_s > f_r$.

In PLR, the output stage is connected in parallel with the resonant tank capacitor. The PLR converters differ from SLR converters in many respects.

(a) PLR converters appear as a voltage source and are better suited for parallel operations.

(b) Unlike SLR converters, PLR converters do not possess inherent short-circuit protection capabilities.

Limitations of the Load Resonant DC-AC Converter

(i) Load resonant converters are ideally suited for constant load applications.

(ii) Since both the resonant elements and the switching devices are connected in power transfer path, the switching devices suffer from high voltage and current stresses.

(iii) The size and weight of LC components become large.

(iv) Better voltage regulation is possible by tuning load close to the resonant frequency.

(v) In order to reduce the output distortion and to achieve a wide range of output voltage, the quality factor (Q) of the resonant tank must be as high as possible.

2.3 Resonant Link Inverters

In resonant link inverters, the resonant network is connected between the source and the inverter bridge. The resonance of this network is utilised to bring the link voltage or current periodically down to zero to create a soft-switching condition. Resonant link inverters are classified according to the type of resonance employed in the link. Primarily, they are known

as resonant ac link (RACL) and resonant dc link (RDCL) inverters.

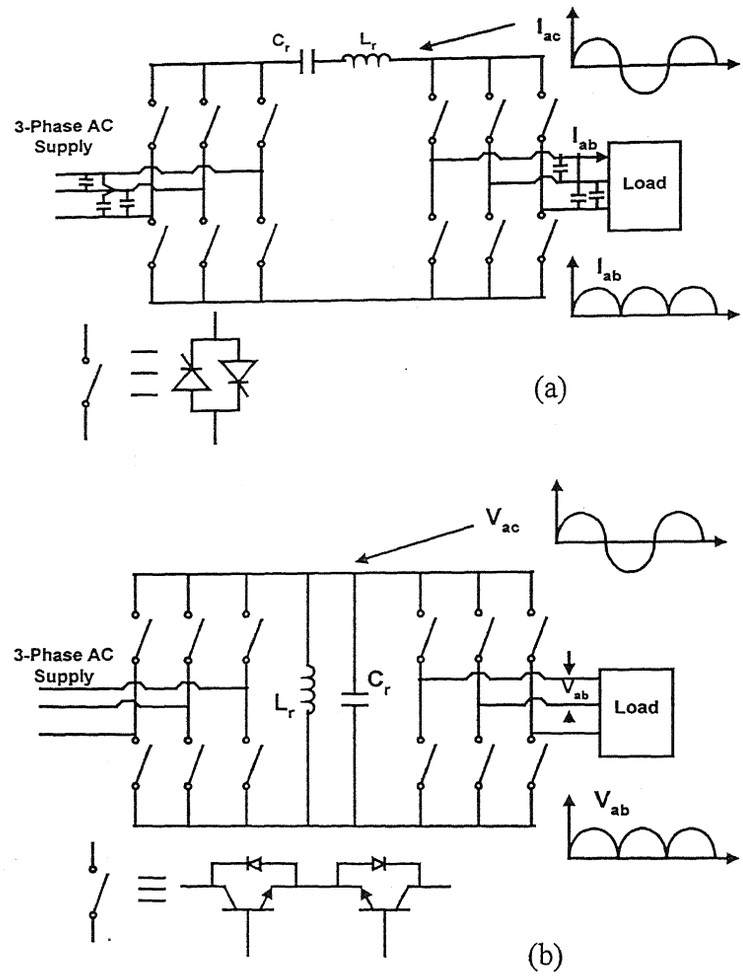


Fig. 2.3. Resonant ac link dc-ac converters
(a) Series resonant ac link (SRACL)
(b) Parallel resonant ac link (PRACL)

A resonant ac link using series resonance was reported by Klaassens [9]. Sul and Lipo [10] reported a resonant ac link based on parallel resonance suitable for an induction motor drive. The circuit diagrams for the resonant ac link using series resonance [9] and the resonant

ac link using parallel resonance [10] are shown in Figs. 2.3(a) and (b) respectively. In series resonance ac link (SRACL) shown in Fig. 2.3(a), the resonant components L_r and C_r are connected in series in the link. Since the link current is bi-directional, the devices used in the supply side and load side converters must have the capability to conduct bi-directionally. The switching devices are turned-on/off naturally at the zero-crossing of the alternating currents realizing ZCS operation. Each switch is realized by connecting two thyristors in anti-parallel as shown in Fig. 2.3(a).

The resonant components are connected in parallel in the case of the parallel resonant ac link (PRACL), as shown in Fig. 2.3(b). The resonant ac link imposes voltages of both polarities in both directions of the inverter devices. In this case, bi-directional devices are used and realized by two self-commutating devices connected in series as shown in Fig. 2.3(b). The switching devices are operated on zero-voltage switching (ZVS). The main shortcomings of the resonant ac link inverter are that it requires a large number of devices and the control circuit becomes quite involved.

2.4 Resonant DC Link (RDCL)

Resonant networks are placed between the source and the inverter. They are classified as (a) series resonant dc link (SRDCL) and (b) Parallel resonant dc link (PRDCL). The circuit schematic block diagrams of SRDCL and PRDCL are shown in Fig. 2.4. Murai and Lipo [11] proposed the concept of SRDCL in 1988 as shown in Fig. 2.4(a). In this scheme, the resonant components L_r and C_r constitute a series resonant link and the inductor L_d is used for biasing purpose. By establishing an appropriate biasing current in L_d, the link current is made unidirectional. The combination of L_r, C_r and L_d produces periodical zero-crossings of current so as to commutate the inverter devices softly. The inverter devices are anti-parallel thyristors without any commutation circuits. However, the bulky biasing inductor makes this topology not very attractive. However, various topologies of inverters have been reported based on this concept [12-15].

The concept of PRDCL was put forth by Divan [16]. The PRDCL inverter is shown in Fig. 2.4(b). In this scheme, a dc bias voltage is provided to the dc link so that the link voltage becomes unidirectional. As a result, the number of unidirectional devices used is reduced as

compared to the SRDCL and the cost and complexity of the power modulator is also further reduced. The simplification of the power circuit makes the resonant dc link very attractive for industrial applications.

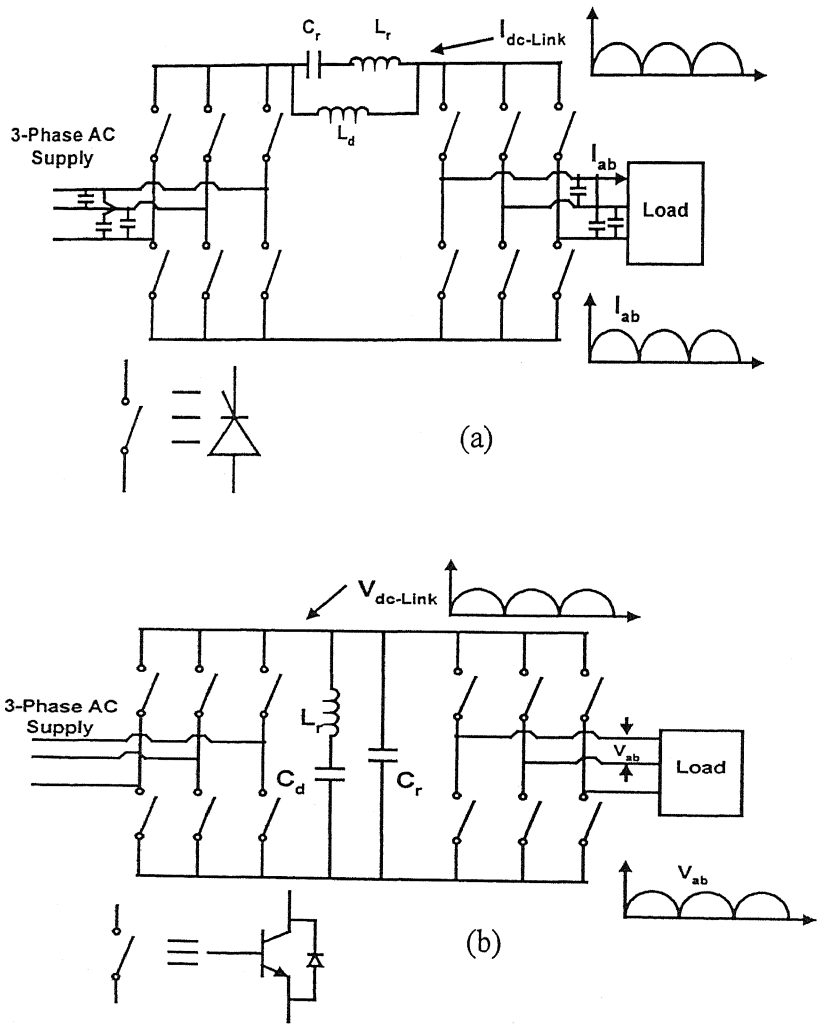


Fig. 2.4. Resonant dc link inverters
(a) Series resonant dc link (SRDCL)
(b) Parallel resonant dc link (PRDCL)

The basic principle of the PRDCL circuit can be explained with a single transistor switch as shown in Fig 2.5(a). The inductor current and resonant link voltage waveforms are shown in Fig. 2.5(b). The circuit consists of the resonant components L_r and C_r. The load is assumed to be inductive having an equivalent series inductance, L_L, which is much larger than the resonant

inductor L_r. The load current I_0 is assumed to be constant during a resonant cycle. The resistance R_r, which is the equivalent series resistance (ESR) of the resonant inductor, accounts for the losses in the resonant circuit.

The operation of the circuit is initiated with the turn-on of the switch S at zero link voltage ($V_r = 0$). The current in the resonant inductor L_r gradually builds up at a rate V_{dc}/L_r. When this current reaches the sufficient value, i_{Lro}, ($i_{Lro} > I_o$), the switch S is turned off with ZVS. The resonance between L_r and C_r produces a voltage pulse as shown in Fig. 2.5(b). The peak voltage of this pulse reaches $2V_{dc}$ approximately before arriving at zero-crossing. For a loss-less circuit, the current in inductor L_r at the end of the cycle will be equal to the initial current i_{Lro}.

However, in a practical circuit, due to losses in R_r, the inductor current i_{Lr} will be less than i_{Lro}. Therefore, to build up the current to the initial value i_{Lro}, the gate pulse to switch S is released at the time instant T_1. Since the dc link voltage is zero and the resonant inductor current is less than I_o, it is the diode D that conducts current in stead of switch S. When the inductor current becomes equal to the load current I_o, the diode turns off soft and the switch S conducts with ZVS. This conduction will continue till end of switching cycle T_p at which the resonant inductor current becomes equal to i_{Lro}. The equations for the resonant link voltage and the inductor current are as given below. From the equation of the link voltage v_r, it is observed that the peak voltage is dependent upon the initial boost current (i.e., $I_d = i_{Lro} - I_0$) in the resonant inductor to meet the losses.

$$v_r = e^{-\alpha t}\omega_0 \; L_r \, I_d \sin \omega_0 t + V_{dc}(1 - \cos \omega_0 t) \qquad (2.1)$$

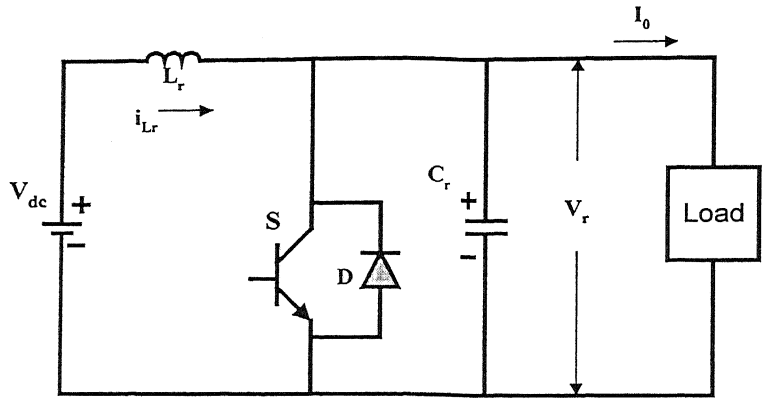
$$i_{Lr} = I_0 + e^{-\alpha t}\left[I_d \cos \omega_0 t + (V_{dc} / \omega_0 L_r) \sin \omega_0 t\right] \qquad (2.2)$$

where $\alpha = R_r / L_r$, $I_d = i_{Lro} - I_0$, $\omega_0 = 1/\sqrt{L_r C_r}$

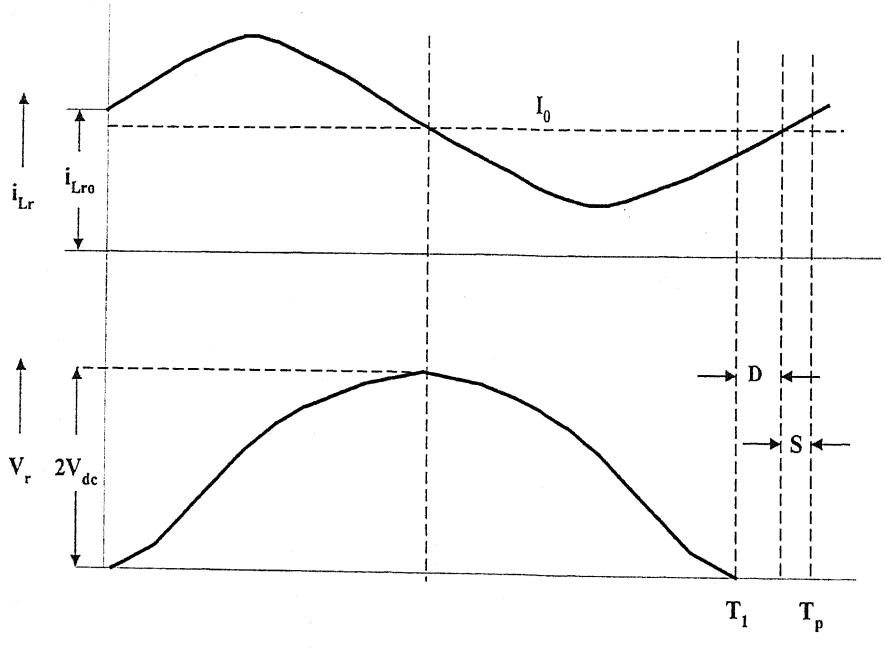
In the basic PRDCL circuit, the load can be replaced by a voltage source inverter. In the dc link, there appear periodic voltage zeros, where the power devices of the inverter can be turned on or off softly. The devices experience voltage stresses, which are greater than twice

the input voltage. The use of devices with higher voltage ratings increases the cost of the power module. Based on this concept, a new topology was proposed by Wold et al. [17].

Though the topology is somewhat different from that in [16], the resonant circuit is not



(a)



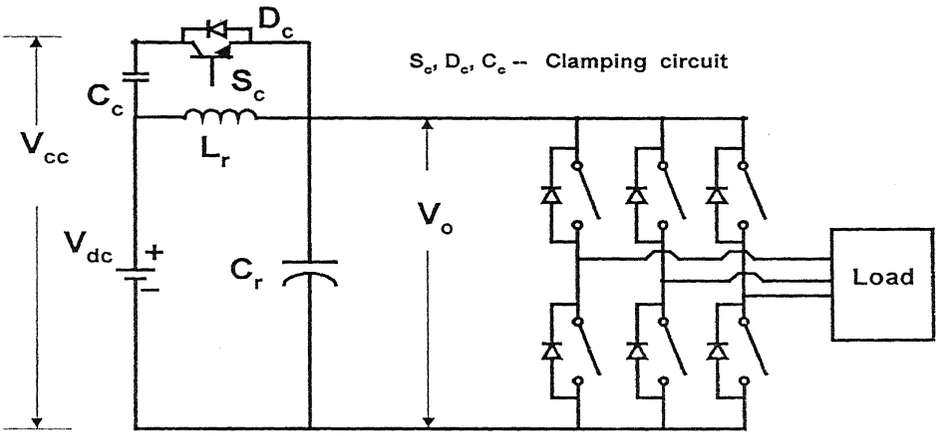
(b)

Fig. 2.5. The basic PRDCL circuit and waveforms across resonant components.
(a) The basic PRDCL circuit
(b) Resonant link voltage and current through resonant inductor current waveforms.

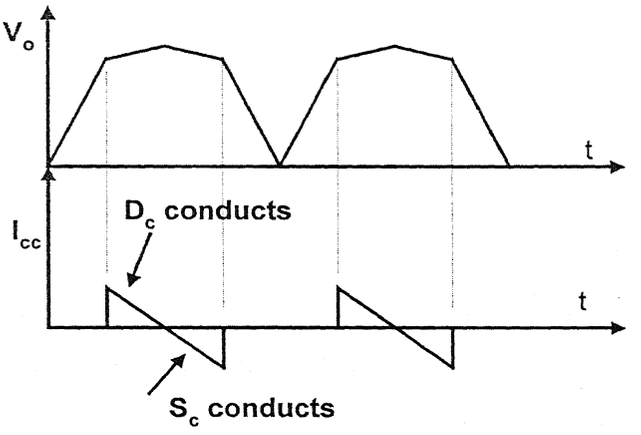
attractive because of the increase in the number of components (four switches, four diodes and three resonant components).

2.5 Actively Clamped PRDCL (ACPRDCL)

Divan et al. proposed the concept of ACPRDCL [18] in 1989. The circuit diagram of ACPRDCL is shown in Fig. 2.6(a). In this case, the active clamping circuit assists to limit the



(a)



(b)

Fig. 2.6. Actively clamped PRDCL circuit and link voltage
(a) ACPRDCL circuit
(b) Link voltage and clamping current (I_{cc}) of ACPRDCL

voltage stresses on the inverter devices to about 1.3 to 1.8 times of the source voltage V_{dc} as compared to the more than $2V_{dc}$ in PRDCL. The clamping voltage is shown in Fig. 2.6(b). The switch S_c, diode D_c and capacitor C_c form the clamping circuit. The link voltage is clamped to V_{cc} with the help of the clamping diode D_c. The clamping switch S_c helps in recovering the charge dumped in C_c such that the average link voltage remains equal to V_{dc}. The clamping circuit also helps in establishing a proper initial current in the resonant inductor L_r for the next resonant cycle. This is achieved by accurately controlling the instant of turn-off of the clamping device S_c. Thus, the shorting of the bus at the zero-crossing is avoided, thereby eliminating the dead period. The clamping voltage V_{cc} can be maintained without the use of auxiliary power supply by properly controlling the clamping device S_c. Based on this concept, the authors reported different topologies in [19-22].

Limitations of ACPRDCL [18]:

(i) High di/dt in every switching cycle. The magnitude of current is a function of 'K' (where $K = V_{cc}/ V_{dc}$). The presence of high (di/dt) increases EMI.

(ii) Variation of link frequency is a function of K and it adds to harmonic contents of the load current.

(iii) The active clamping circuit makes the resonant circuit complex and increases the losses in the link. Additionally, precise control of dc link voltage becomes more difficult.

2.6 Reduced Voltage PRDCL

In order to obtain a stable reduced dc link voltage in ACPRDCL, a simplified reduced voltage PRDCL (RVPRDCL) was proposed by Deshpande and Doradla [23] and its loss calculation was presented [24]. This topology, as shown in Fig. 2.7(a), comprises two more resonant components (L_h and C_h) in addition to the basic PRDCL topology. The resonant switch S_r is closed during every switching cycle to obtain soft-switchings of inverter devices. The two pairs of resonant components ((L_r, C_r) and (L_h, C_h)) are decided in such a way that the resonant frequency of one pair (L_h, C_h) is three times that of the other pair.

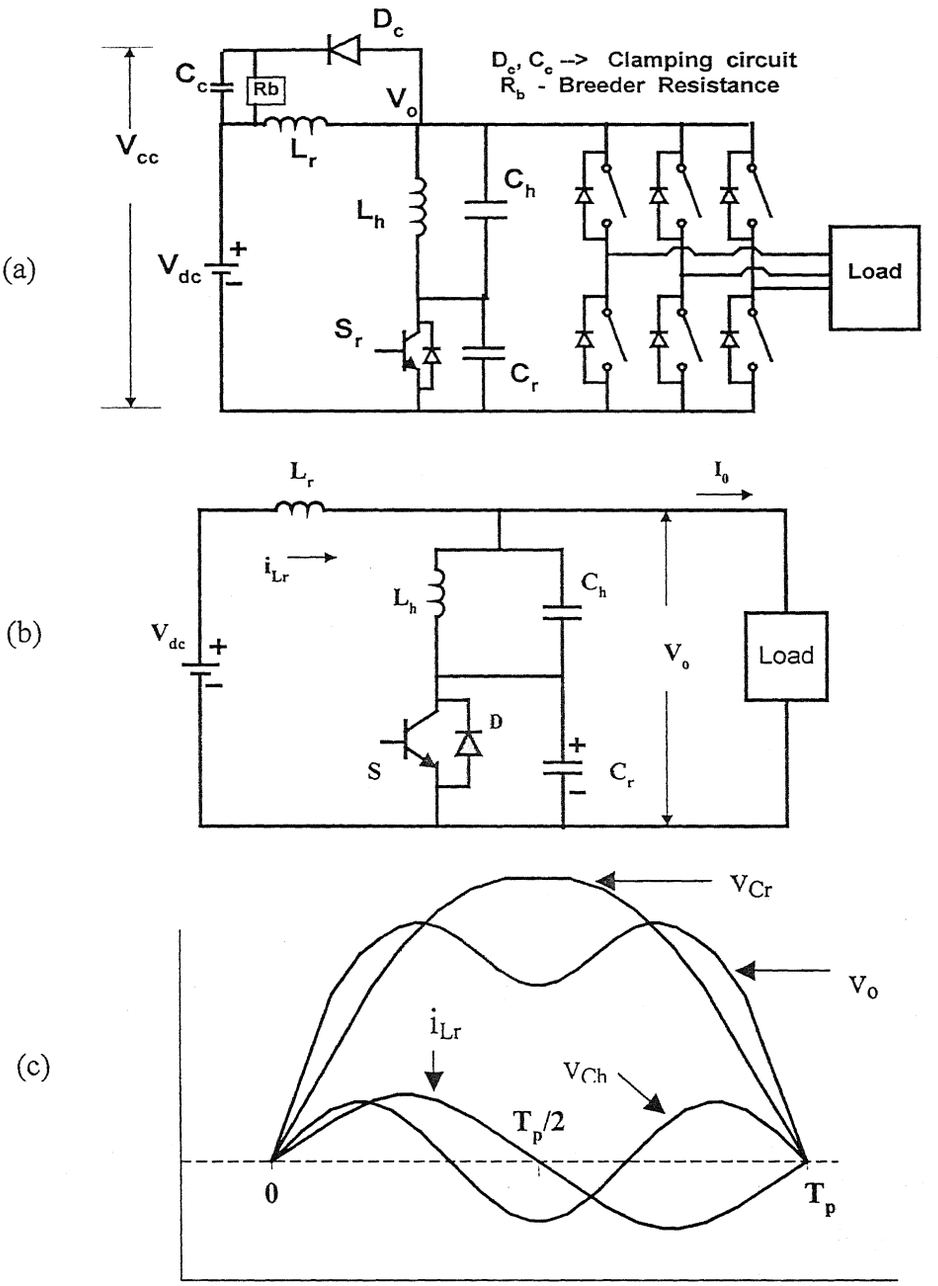


Fig. 2.7. Simplified reduced voltage PRDCL (RVPRDCL) circuit and waveforms.
(a) RVPRDCL circuit (b) Basic RVRL circuit
(c) Resonant link voltage (Vo) and resonant inductor current waveform.

The basic reduced voltage parallel dc link (RVPRDVL) is shown in Fig. 2.7(b). The initial conditions are shown below.

$$i_{Lro} = I_o + I_d$$
$$i_{Lh} = v_{Ch} = v_{Cr} = 0 \qquad (2.3)$$

The operation is similar to that in the basic PRDCL. To initiate the operation, current is provided to resonant inductor L_r to boost I_o so as to compensate for the losses in its equivalent series resistance (ESR). The voltages across the resonant capacitors C_r and C_h are shown in Fig 2.7(c). The combined voltage of C_h and C_r ($v_o = v_{Cr} + v_{Ch}$) appears as reduced voltage across the dc link. It was mentioned that for C_h to C_r ratio 2.0, the dc link voltage can be clamped to 1.5 times of input voltage without the active clamping circuit shown in Fig. 2.7(a). The clamping circuit, which is formed by diode D_c, capacitor C_c and breeder resistance R_b, is further utilized to limit the dc link voltage from exceeding a given value.

Demerits of RVPRDCL:

(i) The circuit has two pairs of resonant components.

(ii) The topology needs a complex control circuit such as a current prediction scheme, which determines the initial boost current in the resonant inductor during each resonant cycle.

2.7 Resonant Transition Inverter

The problems of reduced voltage PRDCL inverters can be overcome by using the principle of resonant transition. In a resonant transition inverter, the input bus voltage of VSI or current of CSI is fixed. The soft-switching condition is implemented by resonating the voltage and/or the current across inverter switches. Ideally, the resonant network should be activated only during the switching transition intervals and completely decoupled from the main power transfer to the load. Frequently, the parasitics of devices can be part of the resonant scheme. However, the resonance energy should be enough to create the soft-switching conditions (ZVS

or ZCS), irrespective of the variations in load. Also, the resonant network should operate according to the controller commanding signals, which are usually provided by a PWM controller. It is also to be noted that the concepts of resonant switch, resonant pole, quasi-resonant, resonant snubber and soft-transition PWM conversion are closely related and can generally be termed as resonant transition when they are applied to dc-ac conversion [25-36,40-45].

The inverters based on the principle of resonant transition technique may be classified into following three categories.

(a) Soft-transition PWM inverter

(b) Resonant snubber inverter

(c) Quasi-Resonant inverter

2.7.1 Soft-Transition PWM Inverter

Vlatkvic et al. [25] proposed the concept of the soft-transition PWM in 1993. The circuit diagram is shown in Fig. 2.8(a). In this case, the bus is clamped at fixed potential and an auxiliary circuit is used to achieve soft-switching operation only during switching transition periods of inverter switches. The operation of the auxiliary switch is synchronized with the PWM control scheme in order to activate the soft-switchings of the inverter switches. The auxiliary diode bridge, the resonant inductor L_r, and the resonant switch S_r create conditions for the turn-on of the inverter switches under the ZVS. The diode D_{fb} is used to feedback the energy of the resonant inductor to the input. All of the diodes are subjected to zero-current turn-on and turn-off, while the main switches are switched at zero-voltage conditions. The operation of this converter is basically the same as that of its conventional PWM counterpart, except during switching transients.

The switching transition between devices connected to phase-a is shown in Fig. 2.8(b). The basic operation is as follows. Assuming that switches S_1, S_2 and S_6 are conducting and phase-a is the most positive terminal, the phase current i_a is flowing out of the converter while i_b and i_c are flowing into it. The soft-switching transition is initiated with all conducting switches (S_1, S_2, S_6) turned off at t_0 under ZVS due to resonant capacitor across

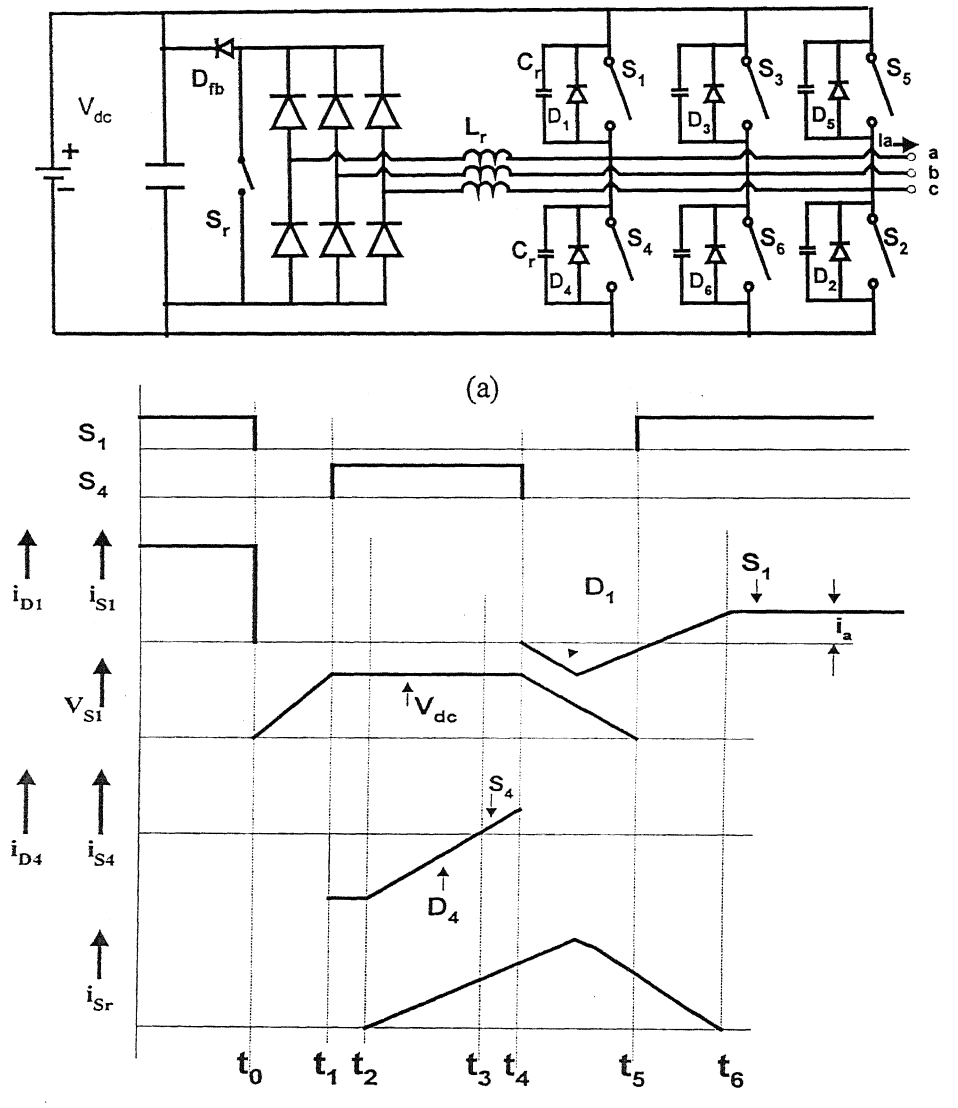


Fig. 2.8. Soft-transition PWM inverter and switching waveforms of devices to connected phase-a.
(a) Soft-transition PWM inverter
(b) Waveforms of soft-switching of the devices connected to phase-a.

each of these devices. As the currents from these switches shift to their corresponding snubber capacitors, the voltage across these switches builds up and becomes equal to source V_{dc} at t_1. Due to inductive load, the three phase currents shift from these snubber capacitors

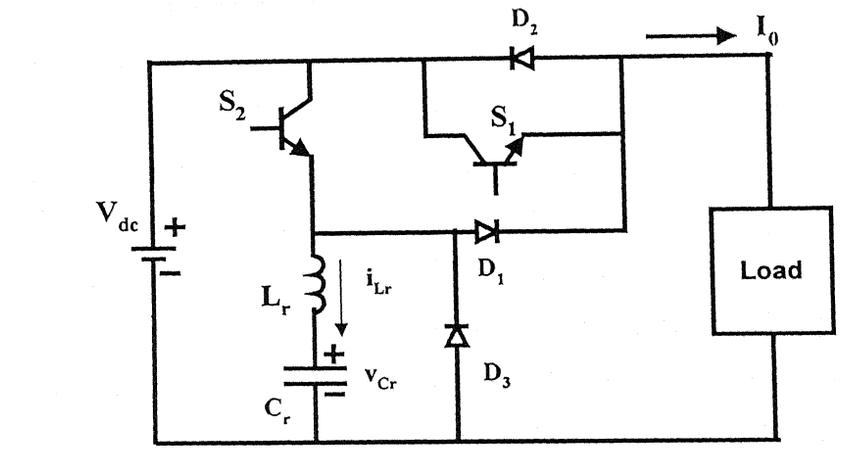
Cr_1, Cr_2, and Cr_6 to the diodes D_4, D_3, and D_5 respectively at t_1. Due to the conduction of these diodes, the gate pulses to switching devices S_4, S_3, and S_5 are released between t_1 and t_2 so as to turn on these devices zero voltage. The auxiliary switch S_r is activated to initiate the zero-voltage transition (ZVT) mechanism at t_2. Therefore, the currents in D_3, D_4, and D_5 are shifted into the auxiliary circuit and charge the resonant inductors L_r in the three phases. The diodes are turned off under zero current at t_3. The switches S_3, S_4, and S_5 begin to conduct at t_3 and add extra currents to all resonating inductors to secure sufficient inductive energy stored in the auxiliary circuit. At t_4, the devices S_3, S_4, and S_5 are turned off with the help of snubber capacitors under zero-voltage conditions. The inductors in the auxiliary bridge resonate with the capacitors of the inverter bridge under the principle of the basic PRDCL circuit given in section 2.4. This resonating voltage results in the conduction of diodes D_1, D_2, and D_6 across the respective switches S_1, S_2, and S_6. Before the currents in these diodes become zero, the gate pulses to switches S_1, S_2, and S_6 are released at t_5 to achieve zero-voltage switching conditions. This scheme has the shortcoming that it requires a large number of components including a diode bridge and three resonant inductors. Based on this concept, some other soft-transition schemes were reported [26-30].

2.7.2 Resonant Snubber-based Inverter

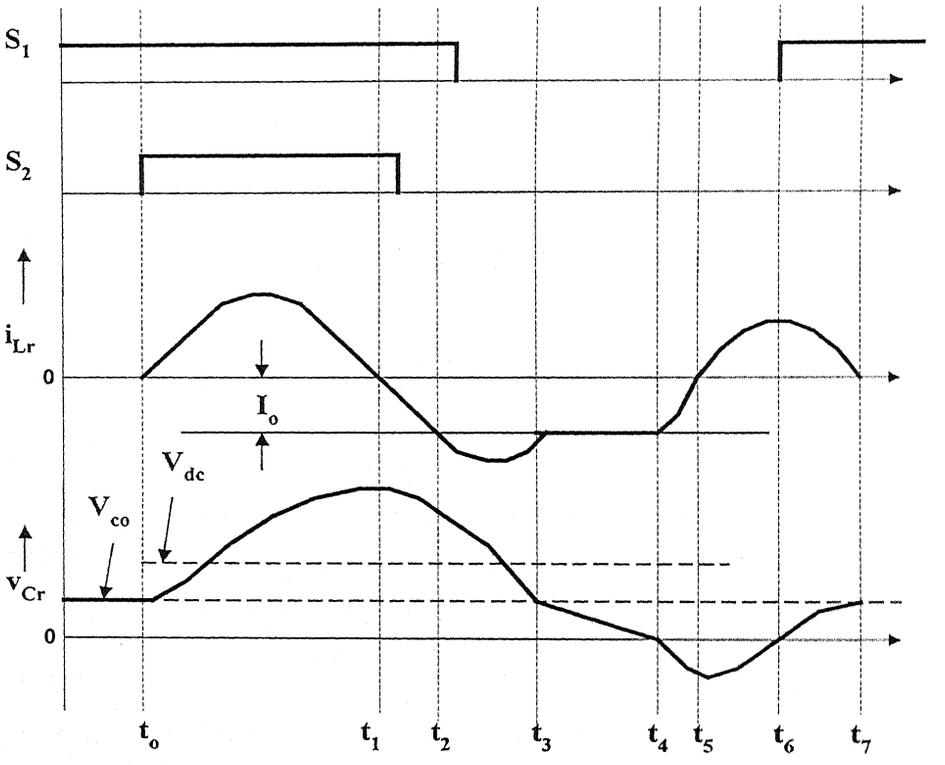
The basic purpose of a resonant snubber inverter (RSI) in [31,32] is to utilize the resonant capacitor across the device to achieve zero-voltage turn-off and the resonant inductor along with an auxiliary switch to achieve zero-voltage turn-on. The three-phase RSI proposed by Lai [32] is shown in Fig. 2.9(a). In order to explain the principle of operation, a single-phase RSI is considered as shown in Fig. 2.9(b). Various modes of operation for a soft-switching transition between inverter switches are shown in Fig. 2.9(c).

Initially, switches S_1, S_2 conduct the load current I_o, which is assumed to be constant. Turning off S_1, S_2 diverts the load current through Cr_1 and Cr_2. As Cr_1 and Cr_2 charge to V_{dc}, Cr_3 and Cr_4 discharge to zero voltage. The load current now shifts to diodes D_3 and D_4. Gating pulses to switches S_3 and S_4 are released at t_0, but these switches do not conduct

by a three-phase voltage source inverter.



(a)



(b)

Fig. 2.14. High frequency inverter-fed induction motor under bang-bang current control. (D. Andrade et al.)
(a) Basic topology of quasi-resonant 3-phase inverter.
(b) Switching waveforms of basic topology

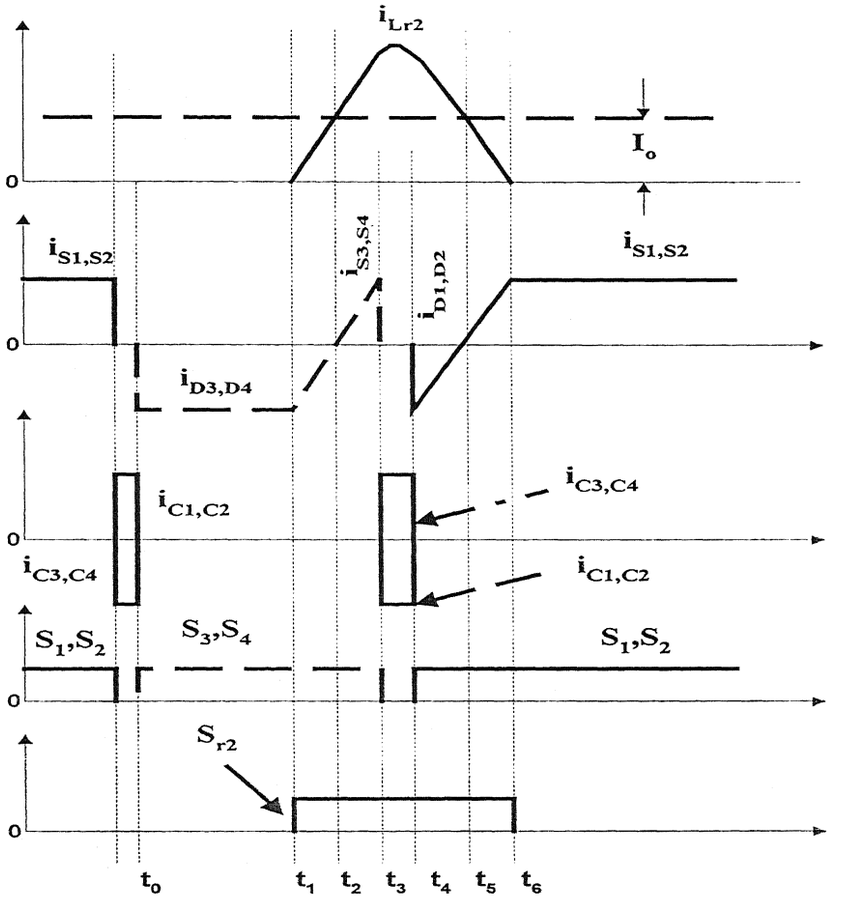


Fig. 2.9 Resonant snubber inverter
(a) Three-phase inverter
(b) Single-phase inverter
(c) Switching waveforms for 1-phase RSI

An auxiliary resonant stage is therefore needed to avoid hard-switching. At t_1, the resonant switch S_{r2} is turned on under ZCS. The inductor current builds up linearly via L_{r2}, S_{r2}, D_{r1}, L_{r1} and the load. The current in diodes D_3 and D_4 gradually reduces to zero at t_2 when the resonant inductor current equals the load current I_o. The current in the resonant

inductor L_{r2} continues to increase above the load current I_o and the excess current above the load current flows through the switches S_3 and S_4 during t_2 to t_3. At t_3, gate pulses to S_3 and S_4 are withdrawn to turn off these devices under ZVS by snubber capacitors C_{r3} and C_{r4}. These resonant capacitors C_{r3} and C_{r4} conduct the current flowing through switches S_3 and S_4. As C_{r3} and C_{r4} charge to source voltage, the capacitors C_{r1} and C_{r2} discharge to zero during time t_3 to t_4. At t_4 , the current in the inductor L_{r2} is still above the load current. The excess current in L_{r2} above the load current flows through diodes D_1 and D_2 and decreases to zero at t_5. Before the current through diodes D_1 and D_2 becomes zero, the gate pulses to switches S_1 and S_2 are released to turn them on under ZVS. During t_5-t_6, the current i_{Lr2} gradually decays to zero and the load current shifts to switches S_1 and S_2. The current in L_{r2} cannot reverse due to the series diode D_{r1}. The limitation of this topology is that the circuit requires one inductor, one diode and one resonant switch in each phase.

2.7.3 The Quasi-Resonant Inverter

In quasi-resonant dc link (QRDCL) inverters, each switching cycle has two parts: resonant interval and non-resonant interval. The resonant interval constitutes a small interval of the switching cycle. During the resonant interval, the resonant network is activated to enable soft-switching transition. This soft-switching transition is implemented by using zero-voltage transition (ZVT) or zero-current transition (ZCT). The circulating energy associated with the soft-switching transition due to resonance is quite small. The resonant components are involved with the load current only during the resonant interval and remain out of operation during the non-resonant interval. The dc link voltage is always clamped to the source voltage in QRDCL inverters. Since the resonant components are involved only during a small interval of the switching cycle, the VA ratings and size of resonant components become quite small compared to those in PRDCL. The QRDCL has two types soft-switching operation.

(i) Zero-current switching QRDCL (ZCS-QRDCL)
(ii) Zero-voltage switching QRDCL (ZVS-QRDCL)

2.7.3.1 The ZCS-QRDCL Inverter

A typical ZCS-QRDCL inverter [33] is shown in Fig.2.10. The topology comprises of two source inductors (L_s), two small resonant inductors (L_r) and a resonant capacitor (C_r). The resonant inductors connected in series with active switches (S_1, S_2) circulate the capacitive energy of C_r in order to create zero-current turn-on and turn-off conditions of switches S_1 and S_2. The switching sequence of this inverter is such that whenever an active switch needs to be turned off, the complementary switch should be turned on first. A series resonance between the output capacitor (C_r) and the two resonant inductors (L_r) releases inductive energy from the outgoing device and the power switch can be turned off at zero current. The resonant inductors ensure the zero-current turn-on of the switches. This topology uses thyristors and hence a low switching frequency is used.

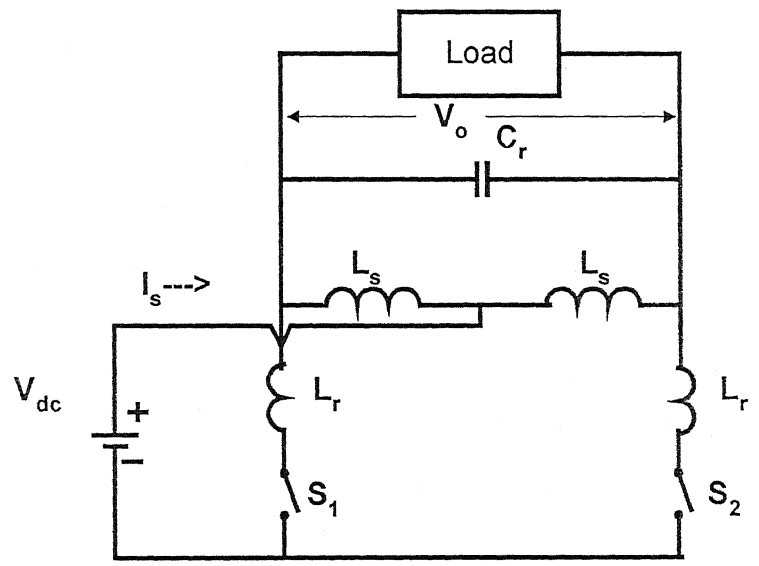


Fig. 2.10. ZCS QRDCL inverter

2.7.3.2 The ZVS-QRDCL Inverter

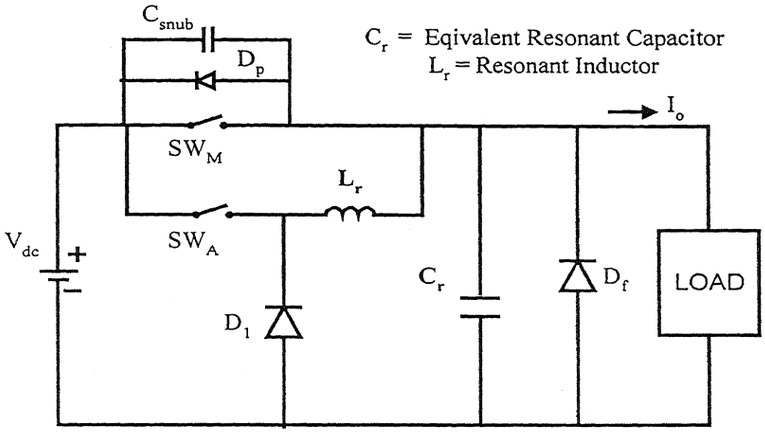
Various QRDCL topologies based on the zero-voltage switching principle have been reported [34-36], [40-45]. The averaging technique for modeling quasi-resonant converters

is discussed in [37]. The authors in [36] suggest the use of IGBT-GTO cascade switches so as to extract a better load performance for high power QRDCL inverters [38].

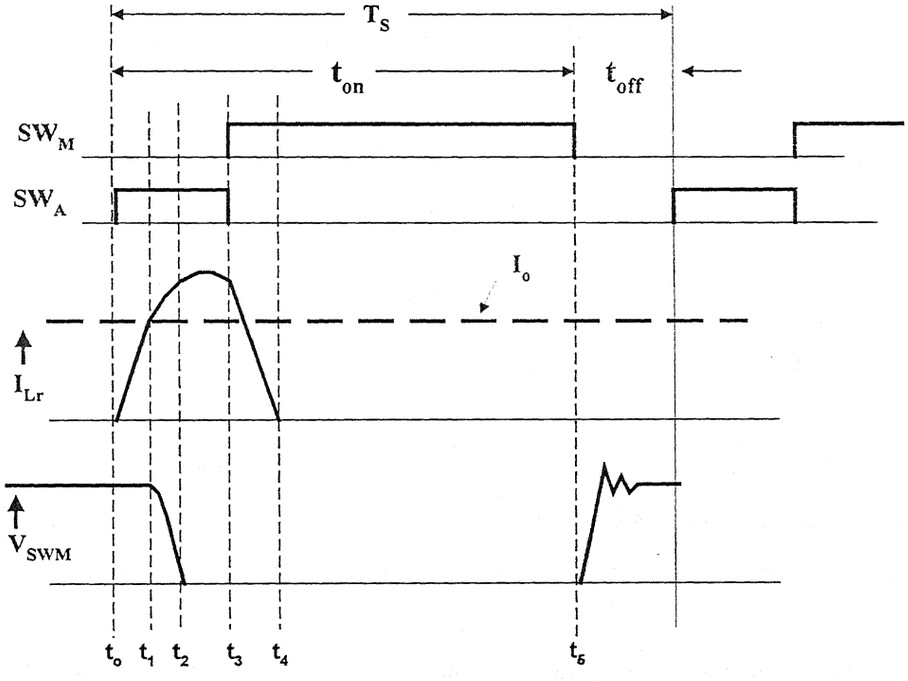
The authors in [34-36,40] propose topologies of QRDCL based on ZVS with PWM control technique. The control technique adopted is to perform PWM operation at any modulation index. Over-modulation and additional switchings to accomplish a given modulation technique are some of the shortcomings of PWM technique. To overcome these problems, the authors in [41] suggest the space vector modulation (SVM) technique. It is reported in [40] that with the use of the SVM technique, the problem of over-modulation index is avoided because of time-ratio control and the number of switchings is reduced with improvement in output waveforms and reduced harmonics. The SVM technique is considered to perform better with the PWM method.

The topology of ZVS-QRDCL was proposed by Lee et al. [41]. This topology is proposed for a load close to unity power factor. In order to explain the basic operation of the circuit, an equivalent circuit (Fig. 2.11(a)) feeding constant load current is considered. Initially, the switches SW_M and SW_A are off and the load current freewheels through diode D_f. The switching waveforms are shown in Fig. 2.11(b). The operation is initiated at t_0 with turn-on of the switch SW_A under ZCS. The current in the resonant inductor L_r starts from zero and the load current I_o is shared by currents in L_r and diode D_f. When the current in the resonant inductor becomes equal to the load current I_o at t_1, the diode D_f turns off because of zero current. At this instant, resonance takes place due to the resonant inductor L_r and the equivalent resonant capacitor C_r. The voltage across the resonant capacitor gradually builds up and when this voltage becomes equal to the source voltage at t_2, the voltage across SW_M falls to zero and the anti-parallel diode D_p gets forward-biased. The gate signal to switch SW_M is released and the gate signal to SW_A is withdrawn at t_3. The inductor energy in L_r feeds back to the source through diode D_1 and D_p till t_4. The switch SW_M is turned on with ZVS, but SW_A turns off hard. SW_M continues to remain on till t_5. The SW_M is turned off with ZVS due to the presence of snubber capacitor across it. The switch SW_M remains off for the duration, t_{off}. The operation repeats at the end of the switching cycle. This topology has two switches with a minimum number of resonant components. The main switch (SW_M) is turned on/off under ZVS, but the auxiliary switch

(SW_A) is turned on under ZCS. It is, however, turned off hard. A modified topology based on this was proposed in [42]. This topology needs an additional capacitor compared to the circuit [41] so as to make the turn-off soft for the device SW_A in Fig. 2.11(a). The load can be replaced by a three-phase voltage source inverter in Fig. 2.11(a).



(a)



(b)

Fig. 2.11. ZVS QRDCL inverter
(a) Basic QRDCL topology (b) Switching waveforms

Filho and Lipo proposed a novel topology [43] that can work for loads of up to 0.88 power factor lagging. This circuit possesses two switches, one resonant inductor, one resonant capacitor across link, and a series-coupled inductor between the source and the dc link as shown in Fig. 2.12.

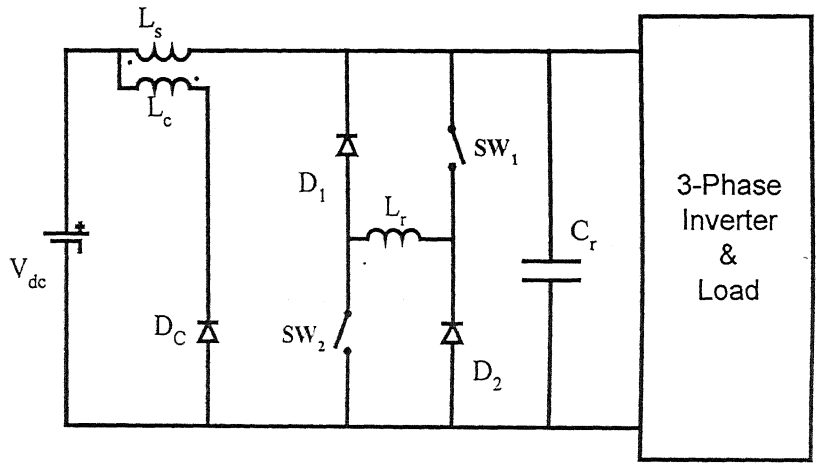


Fig. 2.12. Shunt switch topology

Whenever, a soft-transition of the inverter devices is desired, the shunt switches (SW_1, SW_2) are closed for a small interval. The resonant capacitor voltage discharges through the inductor L_r. This operation causes a notch in the dc link voltage so as to realize a soft-switching operation. During the turn-off of these two switches, the energy in the resonant inductor is transferred to the resonant capacitor, and the energy trapped in L_s is transferred to the coupled inductor L_c and feeds back to the source through L_c and D_c.

A novel topology was reported by Sung and Nam for a VSI-fed induction motor. This topology (Fig. 2.13) fed from a split dc source consists of three GTO switches. The switching frequency is maintained at a low value of 2 kHz. When soft-transitions of the switching devices of the inverter are desired, the link switch S_{Link} is turned off and the

auxiliary switch S_{x2} is turned on. This results in a flow of current through the resonant inductor due to C_r. The link voltage oscillates resonantly to zero. At this instant, soft-transitions of the inverter devices are realized. Before the current through L_r is reversed, the other auxiliary switch S_{x1} is gated to allow the reverse current to oscillate with the resonant capacitor so as to build the voltage across the link for the next switching cycle. The conduction of the auxiliary switches S_{x1} and S_{x2} is overlapped for a small interval and the switch S_{x2} is turned off under ZCS. When the dc link voltage becomes equal to source voltage, the switch S_{Link} is turned on. The energy present in the resonant inductor L_r is fed back to upper half source via S_{x1}, D_{x1}, and diode D_{link}. The author suggests the use of a small inductor in series between L_r and C_r to limit the circulating current in case there is a difference between the source voltage and the dc link voltage. The control technique of the inverters [41-44] is based on space vector modulation. This circuit was tested with a small dc input voltage of 60 V.

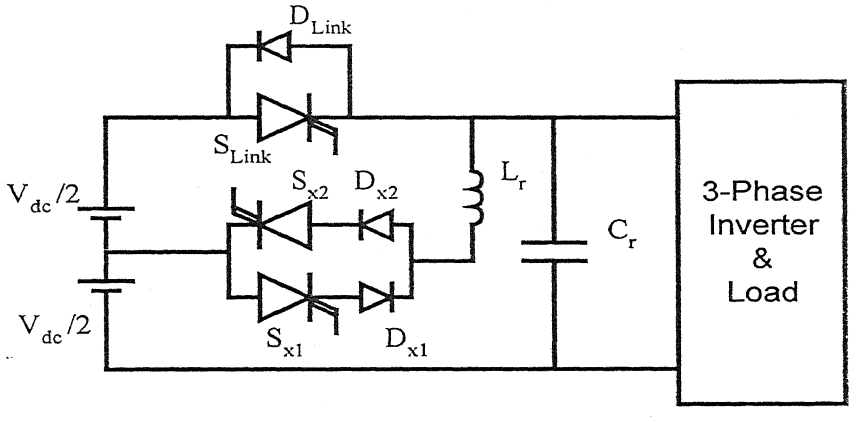


Fig. 2.13. GTO-based inverter topology
(Sung & Nam)

Andrade et al. proposed a new topology [45] for the induction motor load. This topology operates at a comparatively high switching frequency under the bang-bang current controller strategy. The basic operation of this circuit is explained with the equivalent circuit of Fig. 2.14(a) assuming that the load current is constant. The load can be replaced

by a three-phase voltage source inverter.

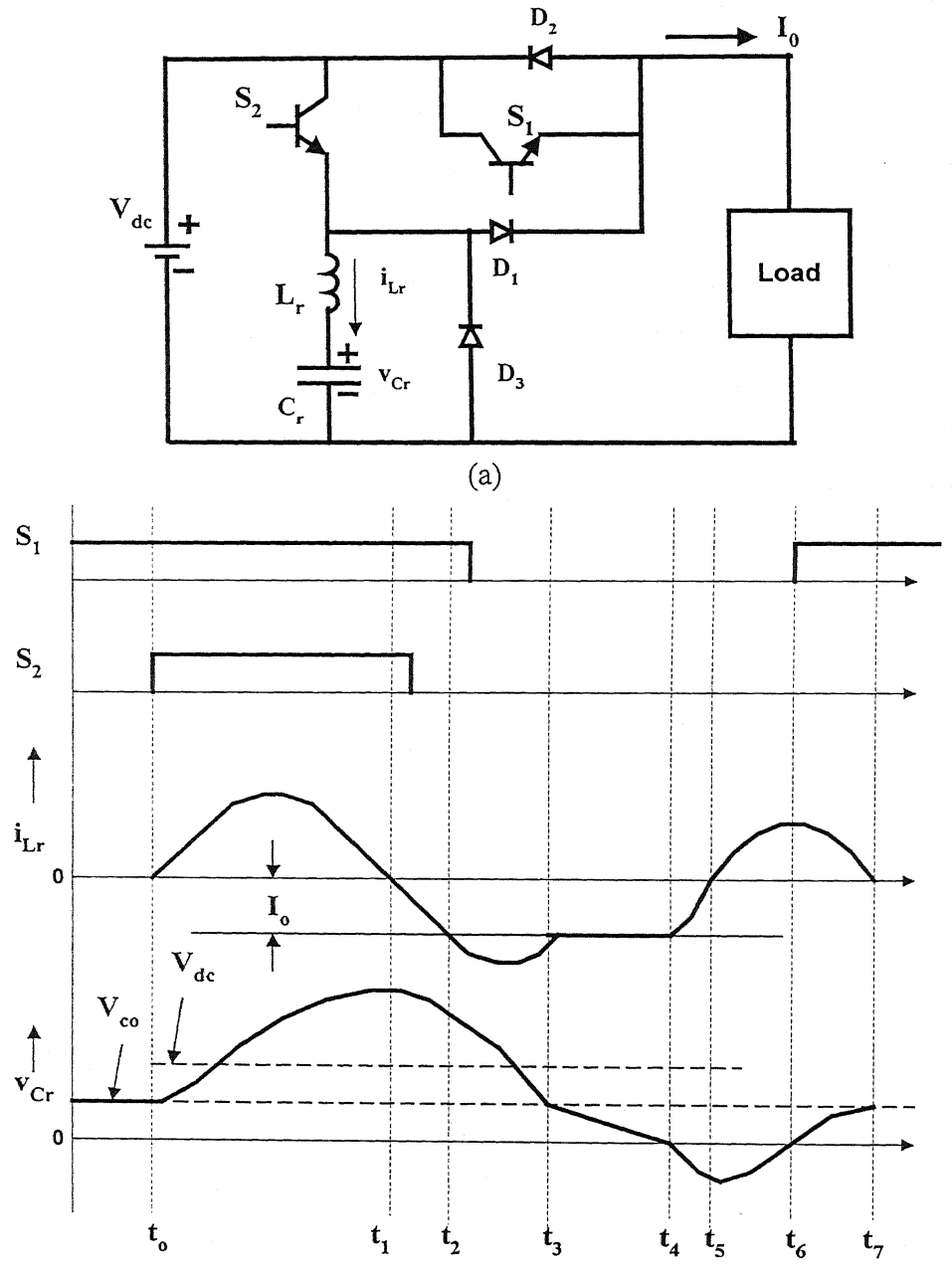


Fig. 2.14. High frequency inverter-fed induction motor under bang-bang current control. (D. Andrade et al.)
(a) Basic topology of quasi-resonant 3-phase inverter.
(b) Switching waveforms of basic topology

The switching waveforms are shown in Fig. 2.14(b). Initially, the switch S_1 conducts the load current and the resonant capacitor C_r is charged to the voltage V_{co}. The operation starts with the turn–on of switch S_2 under ZCS at t_0. The current in the resonant inductor L_r increases from zero and the voltage across the resonant capacitor gradually builds up from the initial value of V_{co}. At t_1, the inductor current passes through natural zero after attaining the peak value and the capacitor voltage reaches a peak value of $2V_{dc}$ approximately. When the inductor current reverses, switch S_2 cannot conduct and is turned off with ZCS during t_1-t_2. The reversal of the inductor current gradually starts supplying the load current through diode D_1 along with switch S_1 ($i_{D1} + i_{S1} = I_o$). The diode current becomes equal to the load current I_o at t_2 supplying the full-load current. The excess current of the resonant inductor above the load current is fed back to the source through diode D_2 and switch S_1 is turned off. The gate signal to switch S_1 is withdrawn during t_2-t_3. The device S_1 turns off soft under ZVS. The resonant inductor current falls to I_o at t_3 after attaining the peak value and the capacitor discharges to V_{co} approximately. At t_3, the diode D_2 is reverse-biased and because of the constant load current I_o, the capacitor discharges to zero at t_4 through diode D_1. During t_3-t_4, the inductor current remains constant. The inductor current now starts decreasing and the capacitor starts to charge in the reverse direction after t_4. The load current is supplied partly by the resonant inductor and the rest is freewheeled through diodes D_1 and D_3. The resonant inductor current falls to zero at t_5 and at this instant the load current completely freewheels through D_3 and D_1. Since capacitor C_r is charged with reverse polarity, it will discharge through inductor L_r and diode D_3. The current in the resonant inductor starts rising with a decrease in capacitor voltage. At t_6, switch S_1 is turned on hard and diode D_1 is reverse-biased for the next switching cycle. The capacitor further reverses its polarity and charges to V_{co} till t_7 where the resonant inductor current falls to zero. The capacitor cannot further discharge because of the reverse-biased diode D_3. It is to be noted that all the switches in the inverter and switch S_1 in the resonant link turn on hard. This topology does not use soft-switching for all devices.

2.8 Conclusion

The various resonant link topologies have been studied and categorized based on soft-

switching operations and resonant conditions. A comparative study of different resonant links reveals that the quasi-resonant dc link topology offers many advantages. Besides, it is simple to implement. It is also observed that the QRDCL inverter with ZVS is easier to implement than the ZCS technique. To the best of author's knowledge, the work related to QRDCL inverter capable of operating with loads of varying power factor (low to high) with complete soft-switching is rather lacking in the literature. Also, soft-switching inverter-fed high performance induction motor drive is not available in the literature. These are taken up for detailed investigation in this thesis. Inverters used in airborne power supplies need to be efficient and small in size, weight, volume. An attempt has been made to study high frequency (fundamental frequency: 400 Hz) QRDCL inverter. To start with, a novel QRDCL inverter topology potentially suited for high frequency power supplies operating with high power factor loads is presented in the next Chapter.

CHAPTER 3

A Quasi-Resonant DC Link Inverter for High Power Factor Load

3.1 Introduction

The comparison of different types of resonant links in Chapter-2 reveals that the Quasi-Resonant DC Link (QRDCL) topology is the simplest among them. It has lower losses. The resonant components are of smaller ratings since they operate over a fraction of a switching cycle. The resonant peak voltage is not allowed to exceed the input voltage.

Most topologies using QRDCL techniques were reported for a VSI [34-36, 40-45]. In [35], the authors proposed three switches in the dc link in addition to the normal bridge inverter. The three-switch topologies were operated under PWM mode as reported in [34], [36]. However, the large number of switches in the dc link for quasi-resonant operation reduces the overall efficiency and reliability. Hence, there is a need to reduce the number of switches and improve the output waveforms close to sinusoidal by incorporating better control techniques.

Wang et al. [41] proposed a two-switch quasi-resonant dc link converter using space vector modulation (SVM) technique for airborne and uninterrupted power supply (UPS) applications. Though the circuit is simple and compact requiring less circulating energy, the auxiliary switch suffers from the turn-off stress. Sung and Nam [44] proposed an improved topology based on [41], but the circuit employed three switches in the dc link.

In this chapter, a new topology is proposed for a VSI. The topology has the following merits when compared to the two-switch topology reported in [41].

- The turn-off of the auxiliary switch is almost without loss.
- The circuit employs a modified SVM suitable for quasi-resonant soft-switched operation.

3.2 Proposed Topology and Modes of Operation

The topology proposed by Wang et al. [41] is modified using an additional capacitor C_{r2} as shown in Fig. 3.1. The simulation of this modified topology reveals two beneficial effects compared to the topology reported in [41]. When the auxiliary switch SW_A is turned on, the dc link voltage is clamped to the source voltage without any circulating current through diode D_p. During turn-off of the auxiliary switch (SW_A), V_{cr2} (voltage across Cr_2) appears across SW_A and this voltage is very small. Thus, the turn-off losses are almost eliminated in the auxiliary switch.

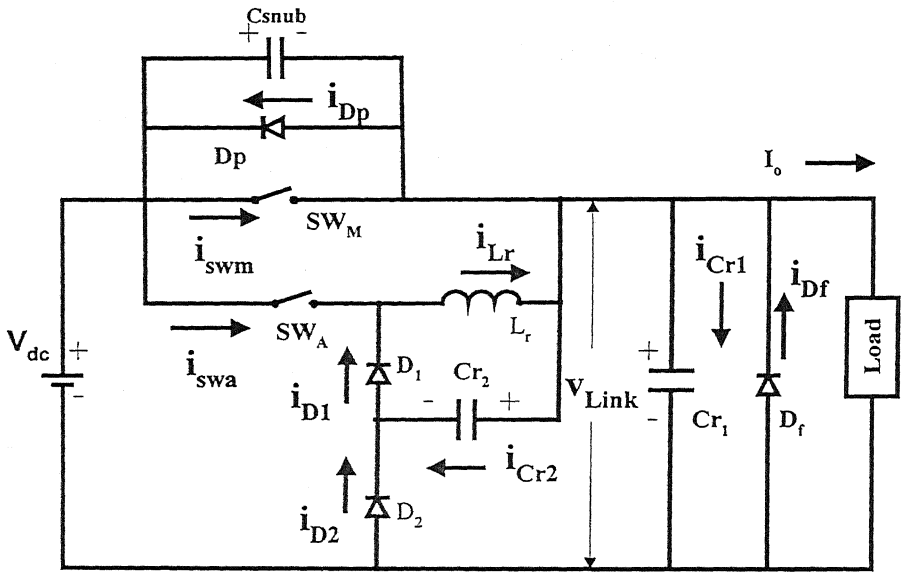


Fig. 3.1. The proposed two-switch topology

The load current is assumed to be constant and the turn-on delay of switching devices of the inverter is neglected. The modes of operation of the circuit of Fig. 3.1 depend on the switching frequency. To start with, both switches are assumed to be in the off state. In this state, if the switching frequency is high, the load current is provided by the discharge current of Cr_2 and the conduction current of the freewheeling diode D_f. On the other hand if the switching frequency is low, the conduction current of the freewheeling diode D_f provides the load current. In the explanation that follows, high switching frequency is assumed and the initial state corresponds to

the former case. The operation of the circuit of Fig. 3.1 is explained for one switching cycle through various modes shown in Fig. 3.2. The control and switching waveforms during various

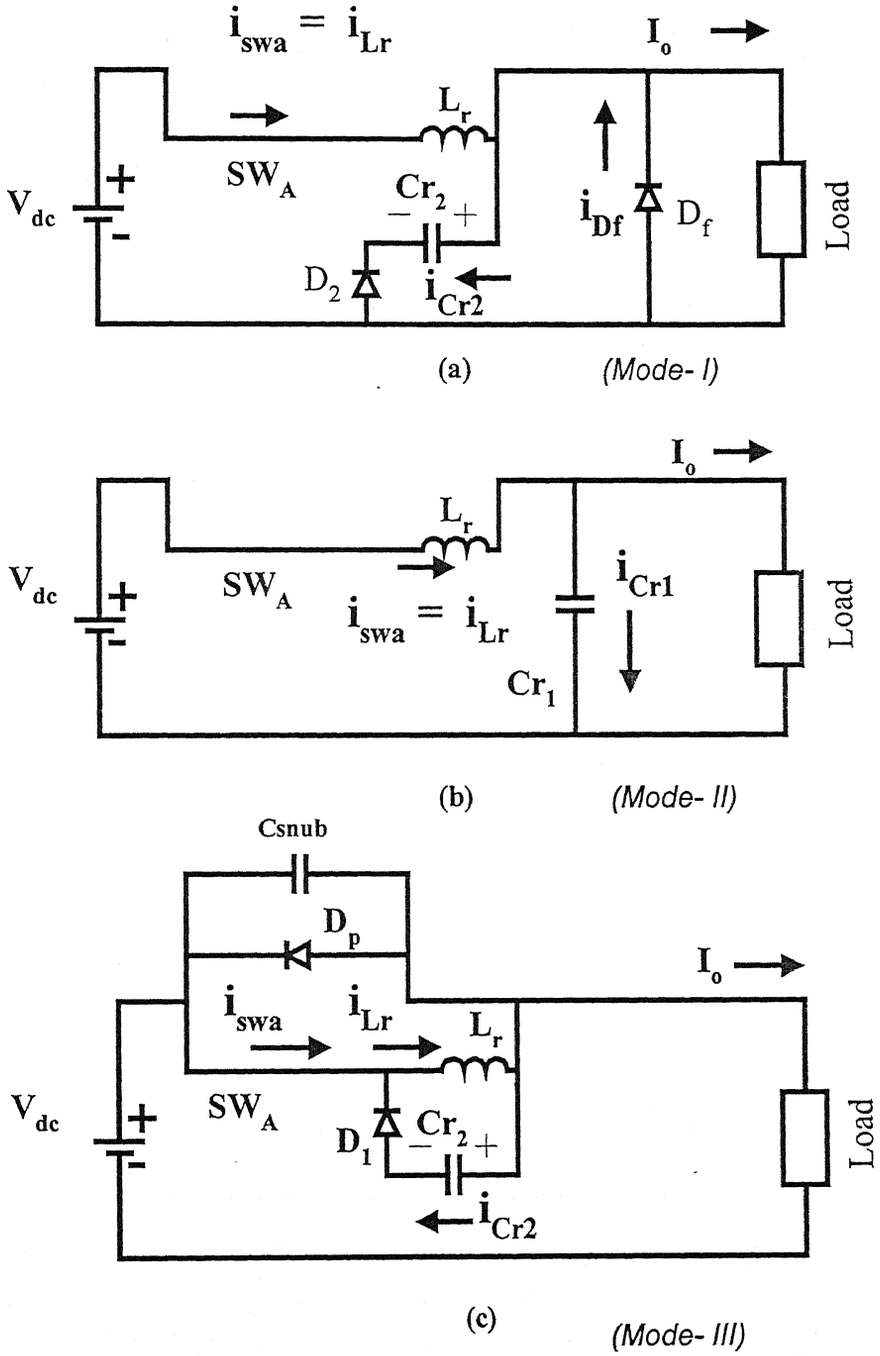
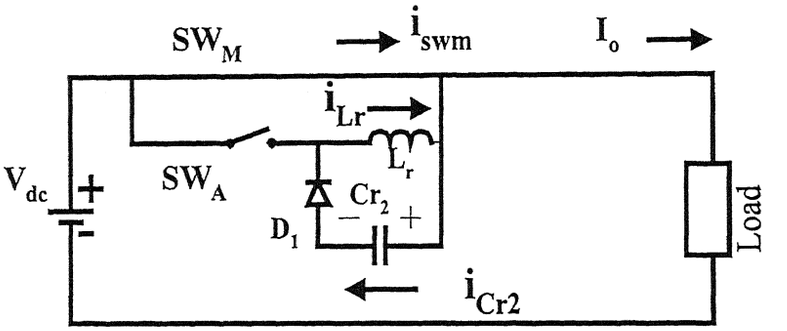
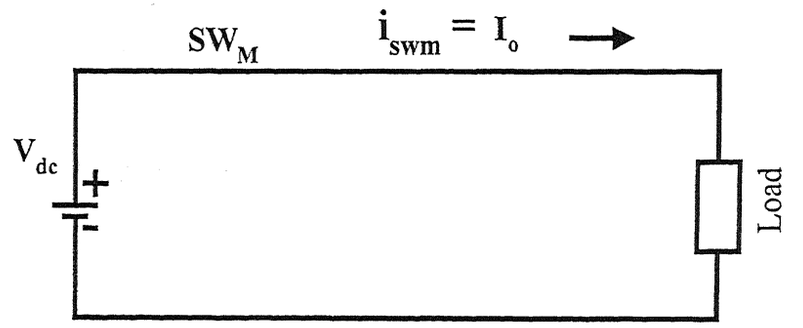


Fig. 3.2 Contd

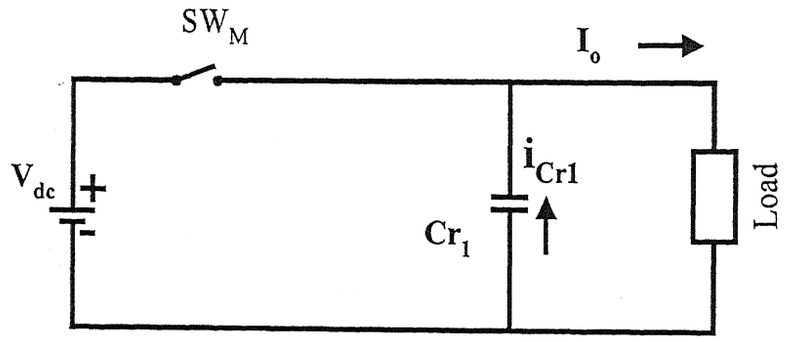
modes of operation at different time intervals are shown in Fig. 3.3.



(d) *(Mode- IV)*

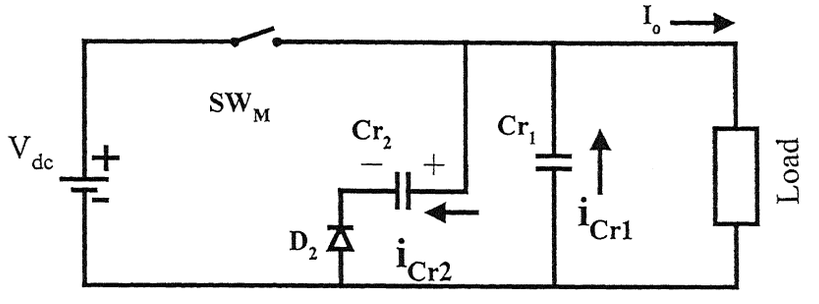


(e) *(Mode- V)*

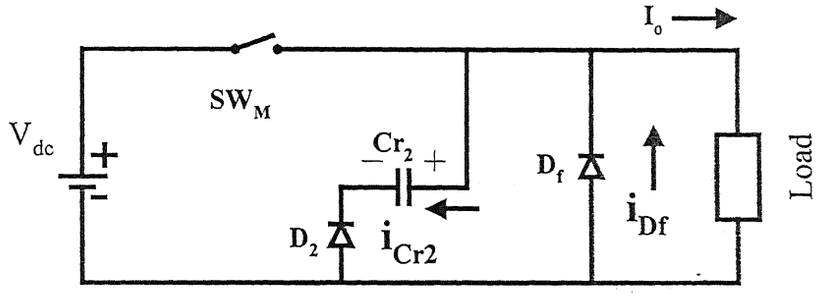


(f) *(Mode- VI)*

Fig. 3.2 Contd.



(g) *(Mode-VII)*



(h) *(Mode-VIII)*

Fig. 3.2. Various modes of two-switch quasi- resonant dc link (QRDCL) topology

(a) Mode- I (b) Mode- II (c) Mode- III (d) Mode- IV
(e) Mode-V (f) Mode- VI (g) Mode-VII (h) Mode-VIII

Mode I (t_0 - t_1): This mode starts with the turn-on of the auxiliary switch SW_A. The equivalent circuit operating in this mode is shown in Fig. 3.2(a). The auxiliary switch SW_A is turned on under ZCS because of the series inductor L_r. The current through the resonant inductor L_r increases linearly while the currents through D_f and Cr_2 fall linearly as the load current is assumed to be constant. This mode ends when the current through the resonant inductor is equal to the load current. The currents through the diode D_f and Cr_2 become zero. The freewheeling diode is turned off.

Mode II (t_1 - t_2): This mode commences from the instant when the inductor L_r carries full load current. The circuit topology corresponding to this mode is shown in Fig. 3.2(b). The resonance between L_r and Cr_1 takes place with the excess current flowing through the capacitor Cr_1 ($i_{swa} = i_{Lr} = I_o + i_{Cr1}$). The voltage starts to build up across the capacitor Cr_1 resonantly. This

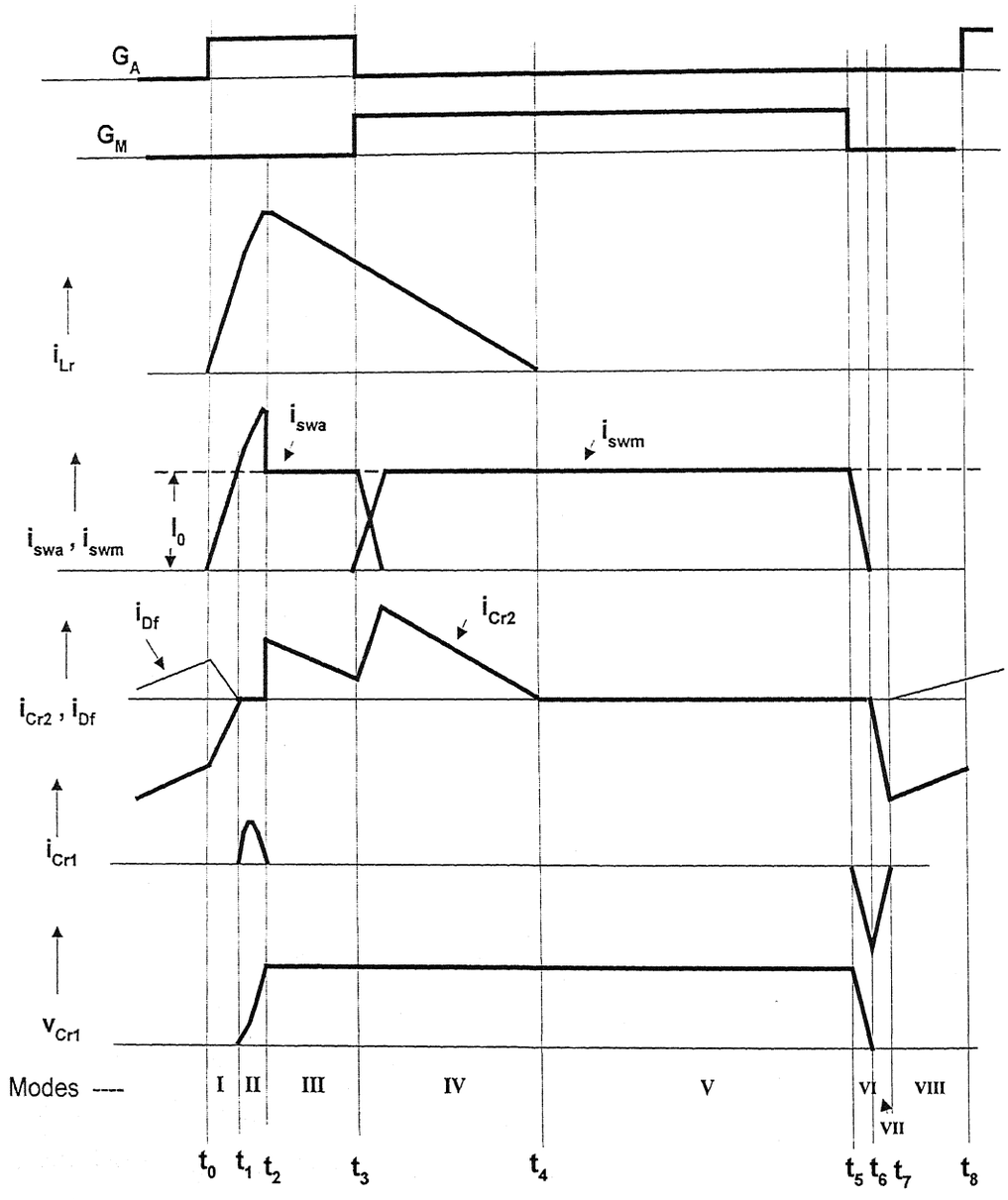


Fig. 3.3. Waveforms of various circuit variables of the proposed two-switch topology for mode-I to mode-VIII.

mode ends as the voltage across the resonant capacitor becomes equal to the source voltage.

Mode III (t_2 - t_3): The circuit topology in this mode is shown in Fig. 3.2(c). When the dc link voltage becomes equal to the source voltage, the diode D_1 becomes forward-biased. With this, Mode-III starts. The resonant inductor provides the load current and the current through the capacitor Cr_2. The current through the auxiliary switch SW_A drops to the level of constant load current while the capacitor current jumps to the value ($i_{Lr} - I_0$). Since the current in the resonant inductor L_r is still more than the load current, it will decay through Cr_2 and D_1. The anti-parallel diode D_p across the main switch SW_M does not conduct since the link voltage is clamped to the source voltage. This mode continues till the instant when the gate pulse from the switch SW_A is withdrawn and the gate pulse to SW_M is released. SW_A is subjected to zero voltage turn-off as D_2 (Fig. 3.1) does not conduct and the voltage across Cr_2 is close to zero. The voltage across Cr_1 is clamped almost to the source voltage by the help of Cr_2.

Mode IV (t_3 - t_4): Figure 3.2(d) shows the circuit topology operating in this mode. The main switch SW_M is turned on and the auxiliary switch SW_A is turned off simultaneously. The current through the main switch increases while at the same time the current through the auxiliary switch decreases. This happens in a very short interval at the beginning of this mode. When the main switch conducts full load current, the current through the auxiliary switch drops to zero. From this instant onwards, the energy stored in the inductor is released to the capacitor Cr_2. The resonant inductor current, thus, flows in the local loop formed by L_r, Cr_2 and D_1. This mode ends when the resonant inductor current discharges to zero.

Mode V (t_4 - t_5): In this mode, the main switch carries the load current and no other components of the circuit conduct as shown in Fig. 3.2(e). This mode ends when the main switch is turned off.

Mode VI (t_5 - t_6): The operating circuit in this mode is shown in Fig. 3.2(f). The main switch is turned off under ZVS because of the presence of the snubber capacitor C_{snub} across the main switch. The capacitor Cr_1 provides the load current. Cr_1 discharges till the voltage across it is equal to the voltage across Cr_2 when this mode ends. It may be noted that the voltage across Cr_2

is very small.

Mode VII (t_6 - t_7): This mode is initiated with the discharging of both Cr_2 and Cr_1 as shown in Fig. 3.2(g). Diode D_2 becomes forward-biased and starts conducting. The discharge currents of both Cr_1 and Cr_2 provide the load current. This mode ends when the current in capacitor Cr_1 becomes zero.

Mode VIII (t_7 - t_8): The operating circuit in this mode is shown in Fig. 3.2(h). This mode starts when the capacitor Cr_1 discharges to zero and the freewheeling diode D_f conducts. The discharging current of capacitor Cr_2 falls and the freewheeling diode current increases. This is the topology that prevails in the beginning before mode-I is started. This mode continues till the auxiliary switch is turned on. It is observed from Fig.3.3 that as the interval of Mode-VIII becomes quite small, the freewheeling diode may not conduct at all. In this case the discharging current of capacitor Cr_2 provides the load current.

From the discussion of various modes of operation of the circuit in Fig. 3.1, it may be noted that the main switch SW_M is turned on/off under ZVS, and the auxiliary switch SW_A is turned on under ZCS and turned off under ZVS. The switching losses in the quasi-resonant dc link are almost eliminated.

3.3 Design of Resonant Components

Before designing the circuit components, the following data are required.

(a) Device critical (di/dt): This can be obtained from manufacturer's specification $(di/dt)_{cr}$

(b) Load current (I_o)

(c) Source input voltage (V_{dc})

Knowing the above data, the circuit components L_r, Cr_1, and Cr_2 are determined from steps 1 to 3 respectively as given below.

Step 1 (Lr): Lr is computed using the condition that the circuit (di/dt) must be less than the device critical (di/dt)

$$(di/dt)_{ckt} \leq (di/dt)_{cr} \quad (3.1)$$

Where $(di/dt)_{ckt} = V_{dc} / L_r$. Once $(di/dt)_{cr}$ is known, the value of L_r can be determined from (3.1).

Step 2 (Cr_1): Cr_1 is computed under the condition that the resonant peak current through C_{r1} must be less than or equal to the load current.

$$Vdc \sqrt{(Cr_1/L_r)} \leq I_o \quad (3.2)$$

Cr_1 is obtained from (3.2) when other parameters are known.

Step 3 (Cr_2): When the auxiliary device is turned on, the resonant peak voltage across Cr_1 must be clamped to the source voltage. The resonance of L_r and Cr_2 will make D_1 conduct whenever the link voltage exceeds the source voltage. This is achieved by designing the resonant period of L_r and Cr_2 to be much higher than that of L_r and Cr_1.

Therefore,

$$\pi\sqrt{(L_r Cr_1)} << \pi\sqrt{(L_r Cr_2)} \quad (3.3)$$

From (3.3), $Cr_2 >> Cr_1$ is obtained.

The simulation studies show that a ratio of $Cr_2/Cr_1 > 1000$ clamps the link voltage equal to the source voltage.

The resonant time period should not be more than 10 % of the switching period T_s for constant switching frequency and variable duty ratio. With this condition, we obtain

$$\pi\sqrt{(L_r Cr_1)} \leq 0.1\, T_s \quad (3.4)$$

Steps (1-3) are repeated with subsequent changes in the values of L_r such that the inequality (3.4) is finally satisfied.

3.4 SVM Control Strategy with Soft-Switching

The proposed quasi-resonant dc link inverter is shown in Fig. 3.4. The circuit operates under the new space vector modulation (SVM) called Modified Space Vector Modulation (MSVM). This is designed for soft-switching operation and it is different from the conventional SVM.

In the conventional SVM technique [34], each fundamental cycle is divided into six sectors as shown in Fig. 3.5. The reference vector (V_r) in each sector is realized by two adjacent non-zero vectors and two zero vectors. There are six non-zero vectors (V_1 - V_6) and two zero vectors

(V_0, V_7). Thus, there are in total eight vectors. The zero vectors are realized by switching on either all upper half or all lower half devices of the three-phase bridge inverter. The durations of two non-zero vectors and a zero vector in any sector are shown in Fig. 3.6 as a function of the angle within a sector. At any instant within a sector, the time intervals $t_1$and t_2 represent the

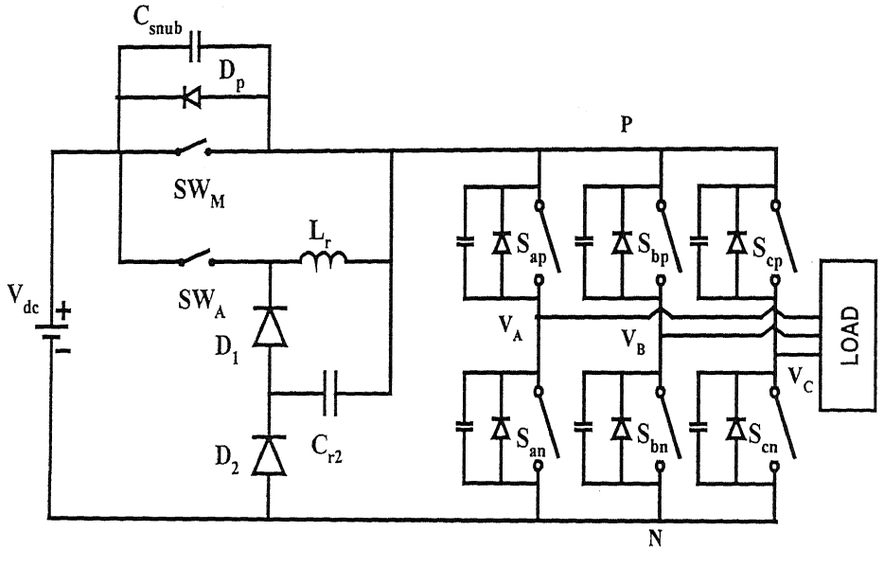


Fig. 3.4. Three-phase quasi-resonant dc link inverter for high power factor load

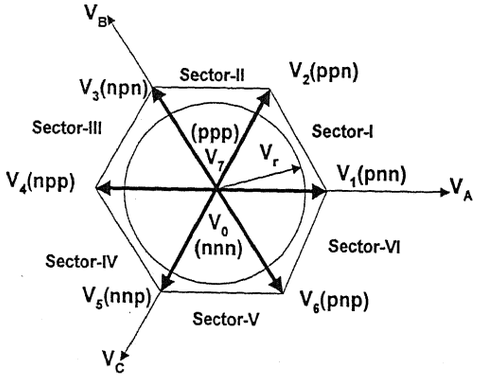


Fig. 3.5. Representation of phase voltage space vector in conventional SVM

durations for the outgoing non-zero vector and the incoming non-zero vector respectively, whereas the time t_z represents the duration for zero vector (V_0 or V_7). In the sector- I, the vector V_1 is the outgoing non-zero vector and V_2 is the incoming non-zero vector for counter-clockwise rotation voltage phasor V_r. Similarly, the outgoing and incoming vectors in other sectors are represented. The sum of t_1, t_2 and t_z is constant and is referred to as the sampling time (T_s). The above SVM technique is applicable to a voltage source inverter using hard-switching. During the operation of zero- vector, the three-phase load terminals are short-circuited. However, the dc link voltage across the bridge remains unchanged because of the voltage of snubber capacitors across the non-conducting switches of the bridge inverter. It is difficult to implement soft-switching (zero-voltage and zero-current switching) in the conventional SVM during the application of zero voltage vector since the link is held at the dc voltage level. To implement soft-switching of inverter devices, it is necessary to have a resonant link with modified SVM technique.

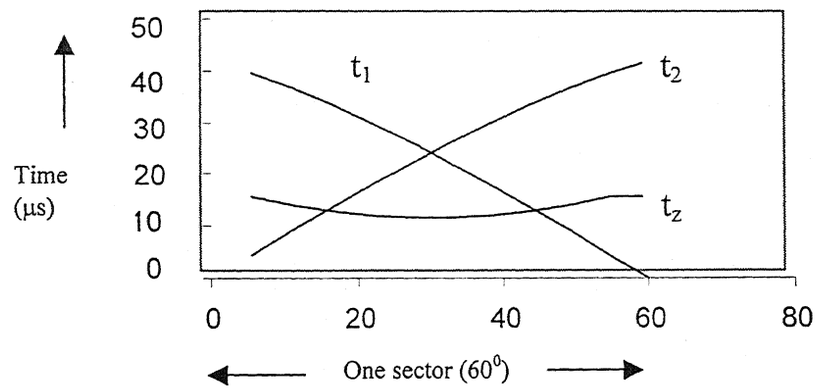


Fig. 3.6. Switching duration of two nonzero and zero vectors in a sector at switching period T_s = 50 μs and modulation index = 0.8

In order to implement the soft-switching with SVM technique, it is necessary to control the dc link appropriately. The zero vectors are initiated by turning off the dc link main switch. The

resonant capacitor appearing across the link is discharged to zero by the load current. The devices conducting in this period contribute to zero vector condition due to zero dc link voltage. This is somewhat different from the conventional zero vectors where the zero vectors are initiated by simultaneously switching either the top half of the devices in the bridge inverter giving V_7 zero vector, or bottom half of the devices in the bridge inverter giving V_0 zero vector. In order to distinguish them from these conventional zero vectors, the zero vectors in the MSVM are represented by Vz_1 and Vz_2, which have different durations. After completion of the zero-voltage vector's duration, the next nonzero vector is initiated by turning on appropriate switches while the dc link voltage is still zero. Hence the inverter switches are turned on/off at ZVS. Then the auxiliary switch SW_A is turned on to bring dc link voltage to the source voltage before the main switch SW_M is closed as explained in Mode-IV vide Fig. 3.2(d). In this way, the new soft-switching for SVM called MSVM is realized. In what follows, this technique is explained for a particular sector.

Each sector is divided into an even number of sampling intervals. The sampling interval is the sampling time ($T_s = 1/f_s$) where f_s is the switching frequency of the dc link switches. The periodic cycle of the dc link switch is maintained at twice the sampling time. Though the switches associated with nonzero vectors operating within the inverter are sampled at $2T_s$, the dc link main switch, which separates input supply from the dc link of the bridge inverter, operates twice for unequal intervals in each repetitive period $2T_s$. Sector-I is considered to explain the operation of the inverter. Similarly, other sectors follow the same principles.

In sector-I, the devices S_{ap} and S_{cn} of the inverter (Fig. 3.4) remain on and the switching takes place between S_{bp} and S_{bn}. The reference vector (V_r) is realized by two nonzero vectors (V_1, V_2) and two zero vectors (Vz_1, Vz_2). The timings of both zero vectors and nonzero vectors during each repetitive period $2T_s$ are determined as follows. The gating pulses for switching devices in the resonant link and inverter are shown in Fig. 3.7.

V_r = Amplitude of the reference vector.

Defining m_i (modulation index)= V_r/V_{dc}

During the first sampling period, T_s

$$t_{11} = (2/\sqrt{3})\, m_i\, T_s \sin(60^0 - \theta_1) \quad (3.5)$$

$$t_{12} = (2/\sqrt{3})\, m_i\, T_s \sin\theta_1 \quad (3.6)$$

$$t_{z1} = (Ts - t_{11} - t_{12}) \quad (3.7)$$

During second sampling period (T_s to $2T_s$)

$$t_{21} = (2/\sqrt{3})\, m_i\, T_s \sin(60^0 - \theta_2) \quad (3.8)$$

$$t_{22} = (2/\sqrt{3})\, m_i\, T_s \sin\theta_2 \quad (3.9)$$

$$t_{z2} = (T_s - t_{21} - t_{22}) \quad (3.10)$$

From (3.5) and (3.8)

$t_1 = t_{11} + t_{21}$

From (3.6) and (3.9)

$t_2 = t_{12} + t_{22}$

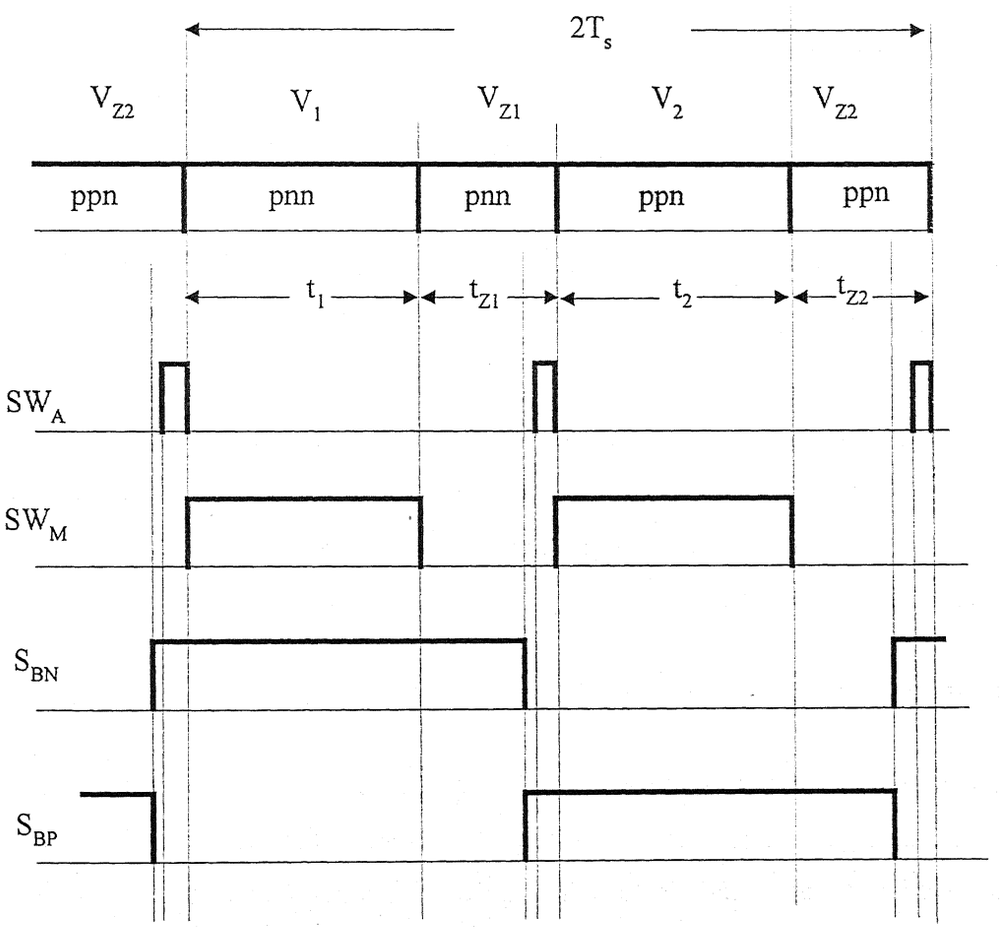


Fig. 3.7 Control technique of implementation of MSVM

where t_1 = Duration of first nonzero vector.

t_2 = Duration of second nonzero vector.

t_{z1}= Duration of first zero vector.

t_{z2}= Duration of second zero vector.

k = Number of samplings in a sector

θ_1 = angle of reference vector at (2 n –1) T_s

θ_2 = angle of reference vector at (2 n) T_s

Where 'n' represents n_{th} times of $2T_s$

(n=1,2,....., k/2..)

In this way, the duration of both zero and nonzero vectors are computed for (k/2) times in subsequent cycles.

In the conventional technique of SVM, the timings of both zero and nonzero vectors during each cycle are based upon sampling period. In this new technique, these calculations of timings are based on twice the sampling period. The main reasons for taking the sampling time $2T_s$ are:

(i) To create a zero vector between the two nonzero vectors without changing switching frequency of the dc link main switch (SW_M).

(ii) At high switching frequency, the difficulty arising in implementing non-zero vectors of small duration ($\cong$ 2 μs) is avoided.

This technique allows a wide range of the switching frequency. Since three switches are involved for both zero and nonzero vectors, the continuity of current is maintained in all phases. Therefore, the soft-switching technique presented here shows improved performance over the technique reported earlier [36].

3.5 Hardware Implementation

The block diagram for the hardware setup is shown in Fig. 3.8. The clock frequency is tapped from the function generator. The clock frequency is then fed to the address decoder that generates eight bit addresses for EPROM. The EPROM is programmed to generate the following pulses in each sector.

(i) Gate pulses for auxiliary (t_{aux}) and main (t_{main}) switches in resonant link.

(ii) Pulse width equivalent to one sector (t_{sect}).

(iii) Pulse widths, $(t_1 + t_{z1})$ and $(t_2 + t_{z2})$. The intervals of nonzero outgoing vector V_1 and incoming vector V_2 are t_1 and t_2 respectively; t_{z1} is the duration of zero vector V_{z1} following the nonzero vector V_1; t_{z2} is the duration of zero vector V_{z2} following the nonzero vector V_2. These intervals are shown in Fig. 3.6.

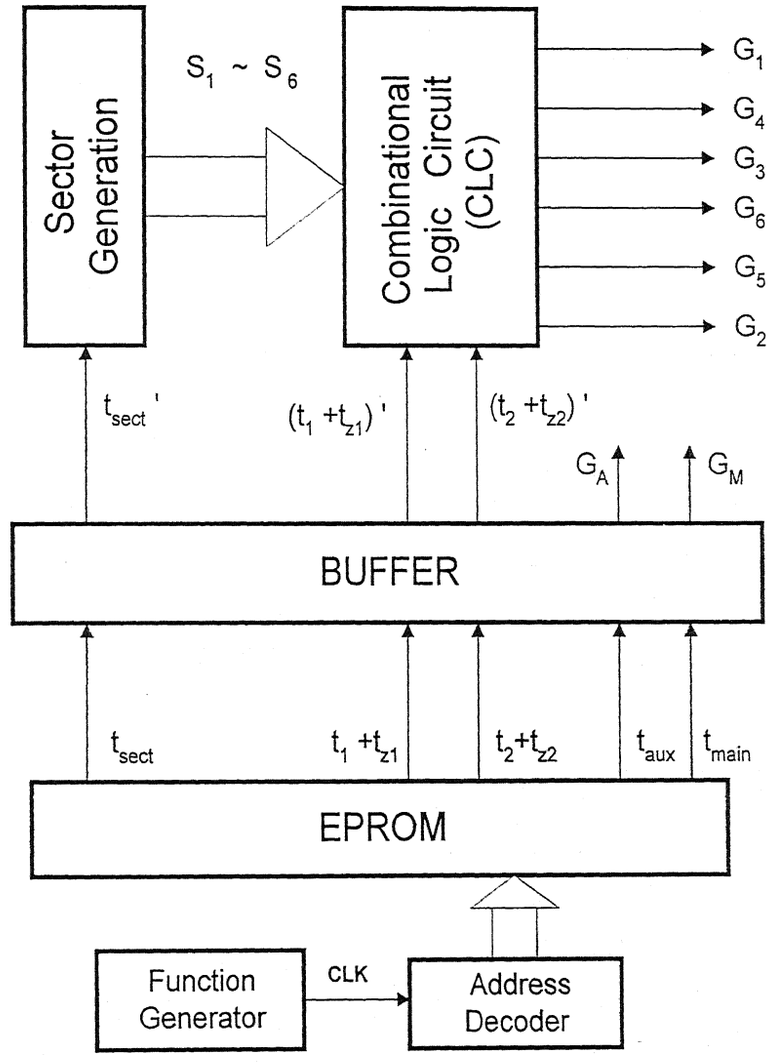
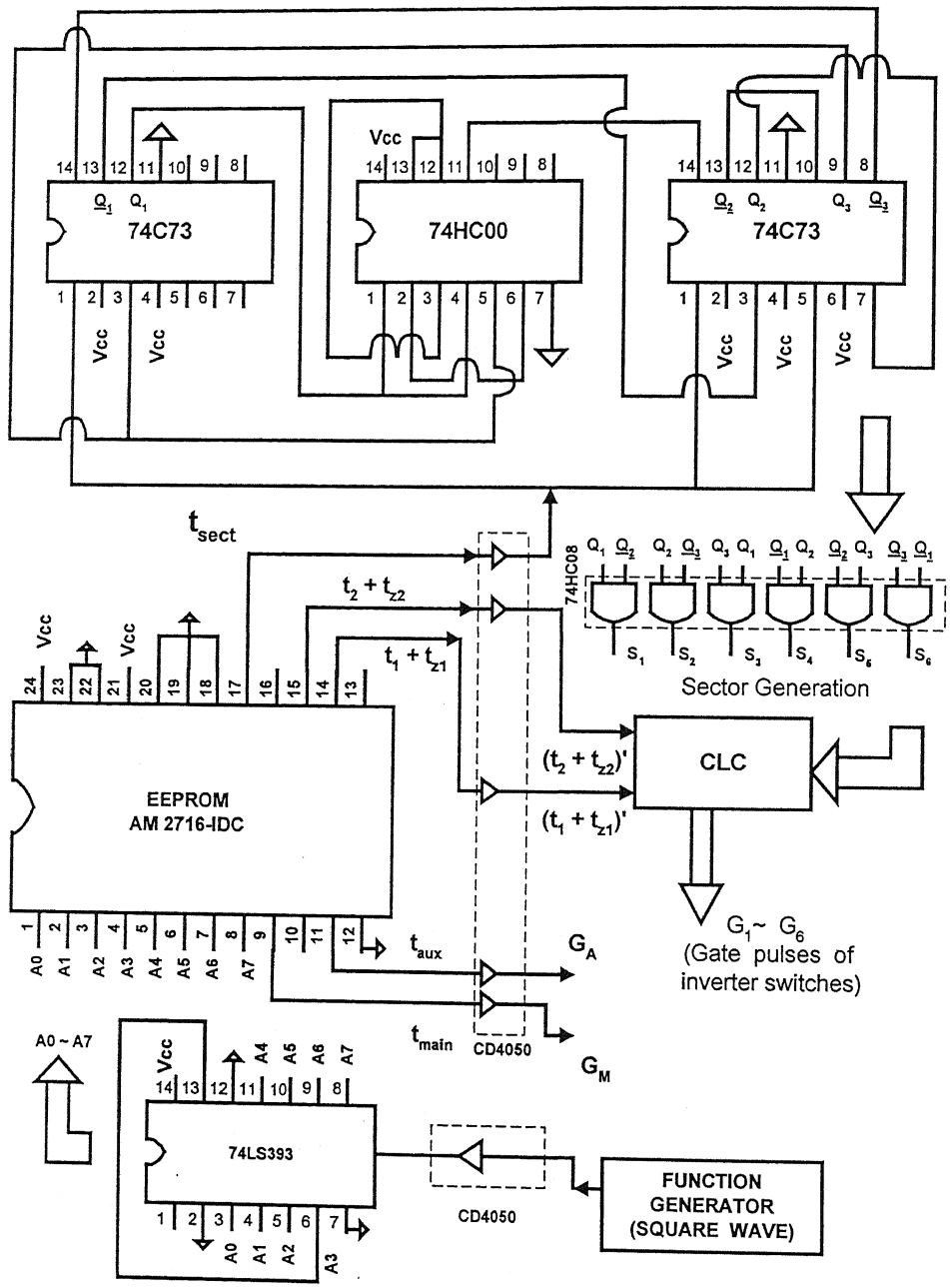
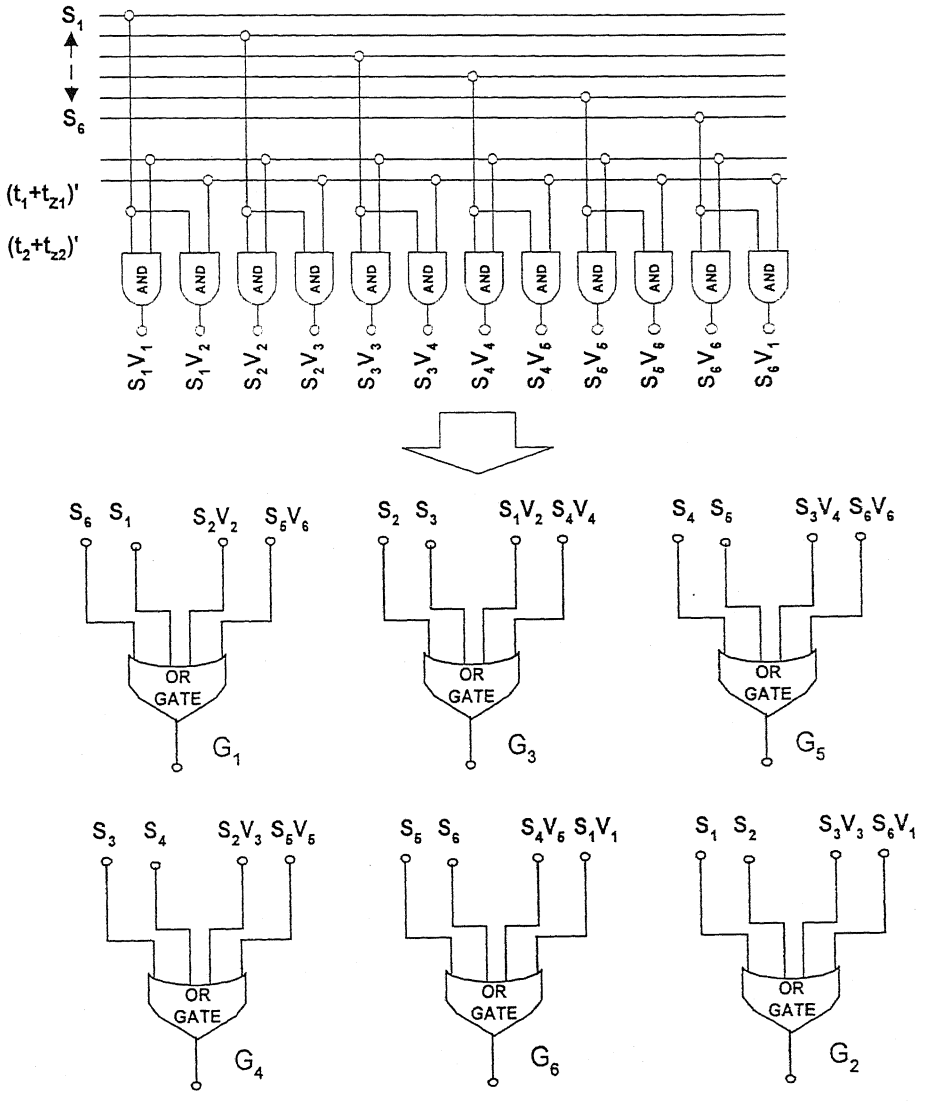


Fig. 3.8. Block diagram of hardware implementation.
t_1, t_2,t_{z1}, t_{z2}, t_{aux}, t_{main}, : Pulse-width signals derived in a sector
t_{sect}: Pulse-width signal equal to a sector
G_1~G_6: Gate signals of inverter switches, G_A,G_M : Gate signals of Auxiliary switch (SW_A) and main switch (SW_M) respectively.



3.9 (a) Detailed pin connection of hardware blocks of Fig. 3.7 excluding CLC



3.9 (b) Combinational Logic Circuit (CLC)

Fig. 3.9. Detailed connection diagram for hardware implementation

The signal 't_{sect}' is used to derive the pulse width of six sectors (S_1, -- S_6) for one complete cycle. These signals for six sectors and buffered signals of (t_1 +t_{z1}) and (t_2+t_{z2}) are fed to combinational logic circuit (CLC) to generate the pulse widths of nonzero vectors and zero vectors for different sectors (S_1, --- S_6). The nonzero vector V_1 (S_{ap}, S_{bn} and S_{cn} in sector-I) is implemented for t_1 with dc link switch closed. The zero vector V_{z1} is implemented for t_{z1} with the dc link switch opened. The status of inverter switches is changed during zero vector intervals (t_{z1}or t_{z2}). Similarly, during the period (t_2+t_{z2}), other nonzero (V_2) and zero (V_{z2}) vectors are implemented with the inverter switches, S_{ap}, S_{bp} and S_{cn}. The CLC generates twelve signals (S_1V_1, --- S_6V_1). The signal S_1V_1 represents vector V_1 in sector S_1. Similarly, the other signals (S_NV_N, N= 1..6) can be defined as shown in Fig. 3.9(b).

These twelve signals are further taken through various logical OR gates and inverters to generate six gate pulses (G_1, -- G_6) of the three-phase inverter of the circuit shown in Fig. 3.4. The gate pulses of switches in the inverter are synchronized with the auxiliary and main switches in the resonant link. G_A, and G_M represent the gate pulses for the auxiliary and main switches of the resonant link respectively as shown in Fig. 3.8. In the proposed scheme, IGBT's are used as switches. The details of pin connections for the hardware implementation are shown in Fig. 3.9. The pin connections of this hardware excluding CLC are shown in Fig. 3.9(a) and the details of CLC are shown in Fig. 3.9(b).

3.6 Simulation Results

The proposed topology along with new SVM technique is modeled and simulated using SABER. The inverter supplies a star-connected three-phase series R-L-Load. The data used for the simulation is listed below.

R_{Load} = 10 Ω/phase, L_{Load} = 400 μH/phase, L_r = 5 μH, V_{dc} = 100 V

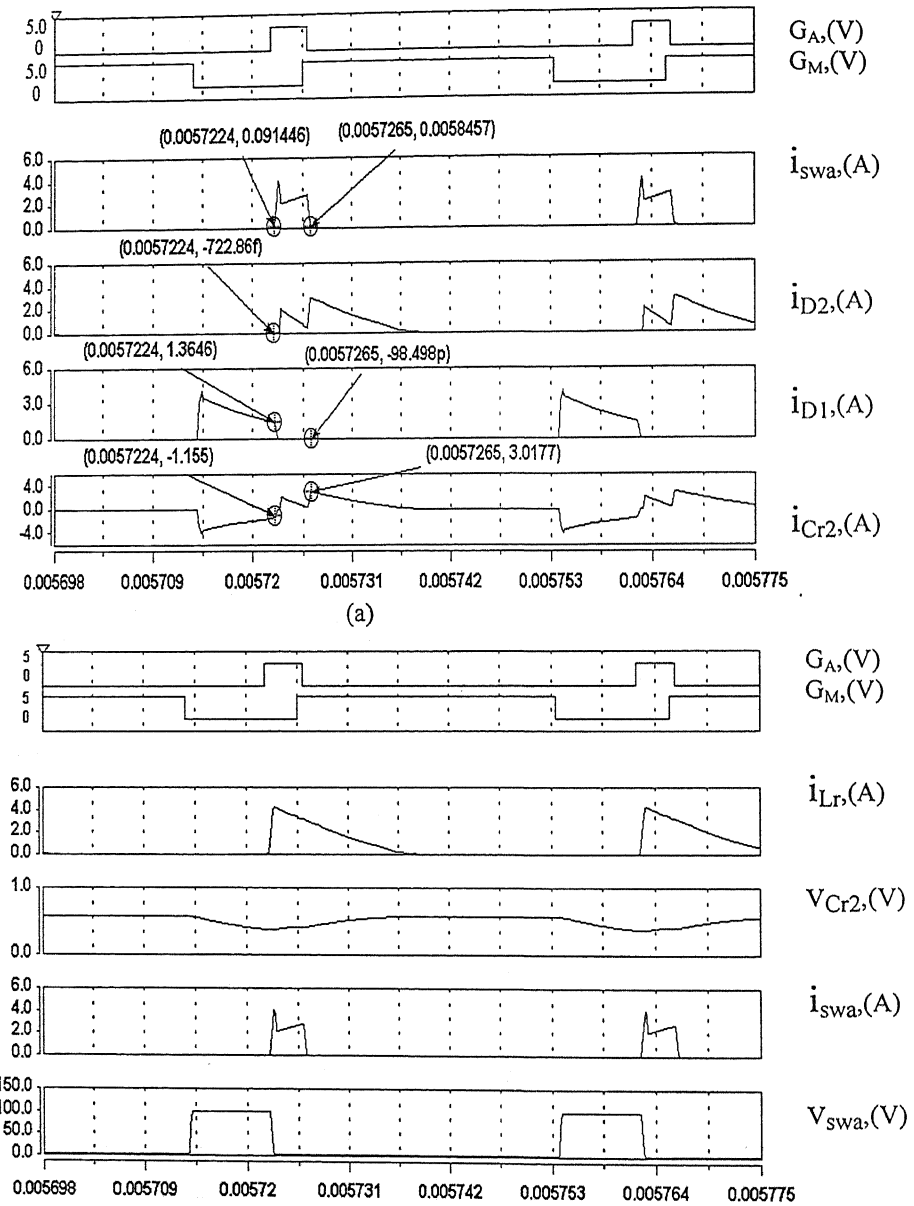
Switching frequency = 25 kHz

Cr_1 (equivalent snubber capacitor across dc link) = 6.6 nF, 1000V Cr_2 = 100 μF, 60V

The source voltage is assumed to be constant. This topology works well for high power factor load (≥ 0.9) due to non-existence of negative current in the dc link. The load inductances are meant to filter the conductive EMI from the output. The modulation index is 0.75 and the fundamental frequency of the inverter is 400 Hz. The results obtained from the SABER simulation at 25 kHz for the soft-switched quasi-resonant three-phase inverter of Fig. 3.1 are shown in Fig. 3.10. In simulation, the gate pulses of the main switch and auxiliary switch have been made to overlap for 0.5 μs to neutralize the effect for turn-on delay time of the main switch SW_M. Without this, it causes a notch in dc link voltage with the turn-off of the switch SW_A, because the resonant capacitor Cr_1 across the link discharges faster than turn-on delay time of the SW_M. There is no adverse effect because of this overlapping of gate pulses. It has been observed no energy circulation in anti-parallel diode D_p of switch SW_M due to overlapping of the gate pulses.

From the simulation results of the current through and voltage across the auxiliary switch SW_A as shown in Fig. 3.10, SW_A is turned on under ZCS due to presence of the resonant inductor L_r in series with the device and the diode D_1 does not conduct. During switching off of the auxiliary switch, it is found that the diode D_2 does not conduct and the capacitor voltage V_{Cr2} appears across the auxiliary switch. Since the capacitor voltage V_{Cr2} is very small in the order of 1 to 2V, the auxiliary switch can be considered to be turned off under ZVS. With Cr_2, any rise in the dc link voltage circulates a current through L_r, Cr_2 and D_1 and thus, the link voltage is clamped to the input voltage without any circulating energy through diode D_p. There is no current flowing through D_p as may be seen in Fig. 3.10.

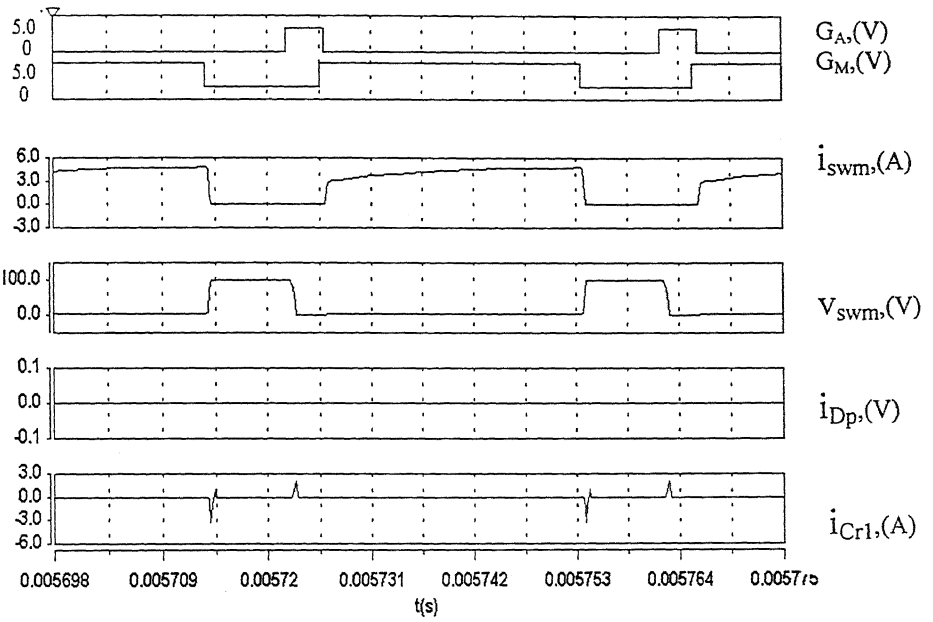
From the waveforms of current and voltage of the main switch in Fig. 3.10, it may be noted that SW_M is turned on/off under ZVS. When both main and auxiliary switches are turned off, the link voltage discharges to zero. This ensures soft-switching operation of the switching devices of the inverter. The simulated phase current and line-to-line voltage using the proposed modified space vector modulation with soft-switching (MSVM) are shown in Fig. 3.11. The steady-state waveform of the phase current departs from sinusoidal comprising of harmonics. This may be due to low inductance in the load circuit and low switching frequency.



(a)

(b) **t(s)** ---

Fig. 3.10. Continued



(c)

Fig. 3.10. Waveforms of different variables of Fig. 3.1 obtained from simulation study at 25 kHz.
G_A, G_M: Gate pulses of SW_A and SW_M.

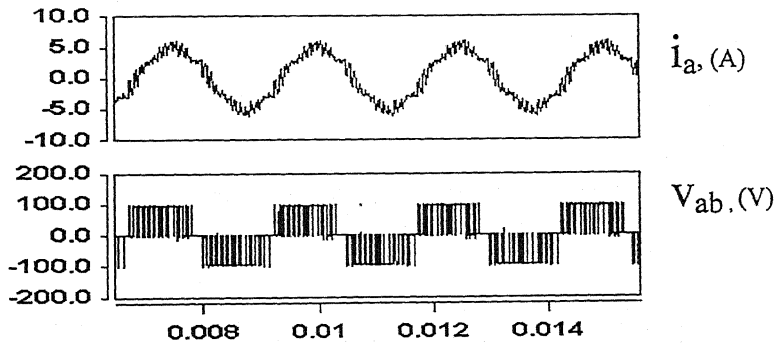


Fig.3.11. Simulation result showing phase current (i_a) and line-to-line voltage (v_{ab}) waveforms of Fig. 3.5 using modified space vector modulation with soft-switching.

To improve the steady-state phase current waveform, the topology is again simulated at a higher switching frequency of 38.5 kHz using MSVM. The various pulse widths of signals for switching devices derived in a sector and the corresponding link voltage are shown in Fig. 3.12(a). As the main switch is opened, the link voltage passes through zero voltage level. The

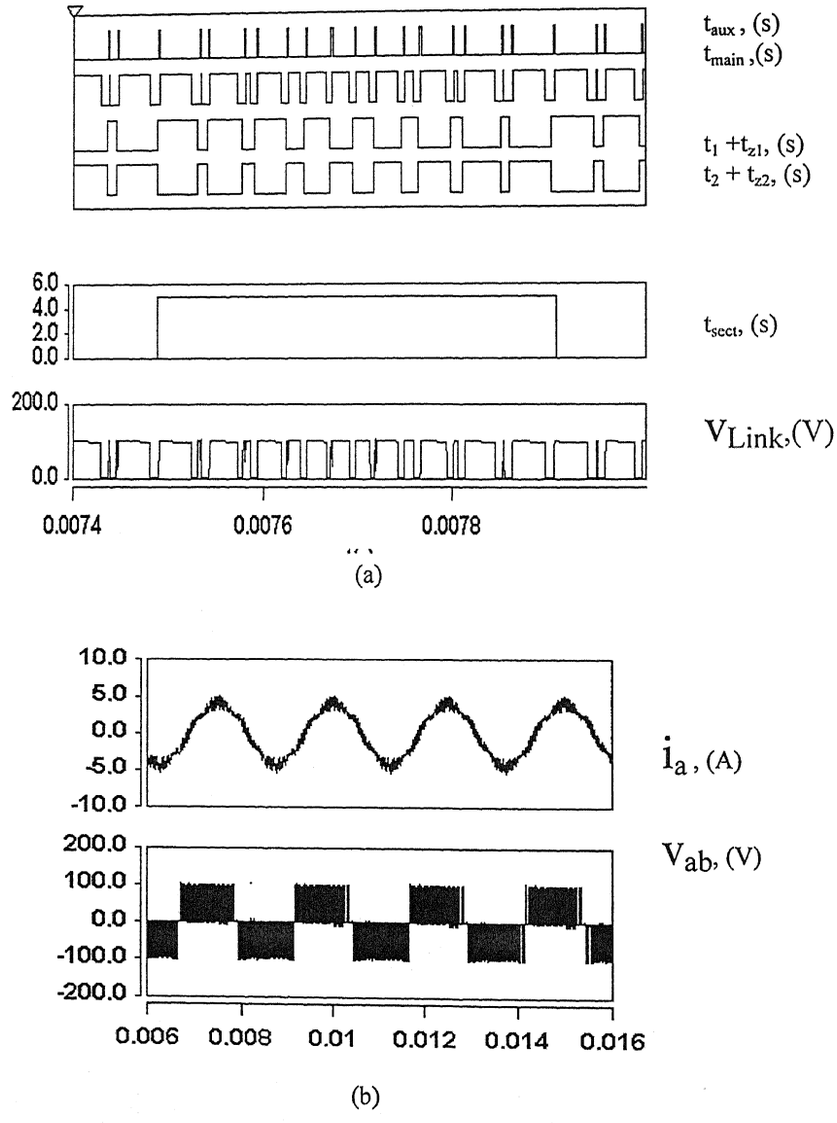


Fig. 3.12. Simulation results at 38.5 kHz switching frequency (R_{Load} =10 Ω , L_{Load} = 400 μH)
(a) Pulse width of signals derived in a sector (t_{aux} , t_{main}, t_1+t_{z1}, t_2+t_{z2} , t_{sect}) and dc link voltage (V_{Link})
(b) Phase current (i_a) and line-to-line voltage (V_{ab})

status of switching devices of the inverter circuit is changed ensuring soft-switching operation. The steady state waveforms of phase current and line-to-line voltage are shown in Fig. 3.12(b). There is an improvement in the waveforms when compared to the same at a lower switching frequency as shown in Fig. 3.11. Further improvement in the waveforms is obtained with increased load inductance as depicted in Fig. 3.13 with the same switching frequency 38.5 kHz, modulation index 0.75, fundamental frequency = 400 Hz. The dc link current is found to be positive as shown in Fig. 3.13.

The auxiliary switch SW_A is turned on under ZCS and turned off under ZVS. The main switch SW_M is turned on/off under ZVS. The switching devices of the inverter are operated under ZVS.

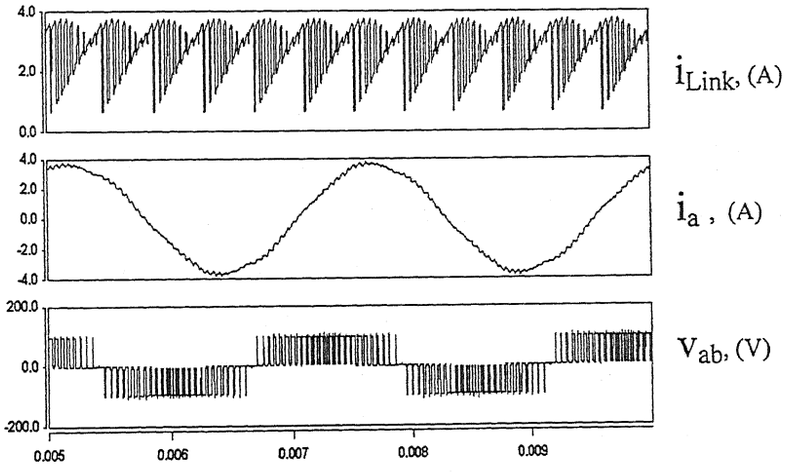


Fig. 3.13. Simulation results at 38.5 kHz switching frequency
(R_{Load} =10 Ω, L_{Load} = 2.3 mH)
Fundamental frequency = 400 Hz
Dc Link current (i_{link}), Phase current (i_a) and line-to-line voltage (V_{ab})

3.7 Experimental Results

Initially, the experiment was conducted at 25 kHz by data acquisition card connected to PC as reported in [42]. The simulation and experimental waveforms of gating pulses of auxiliary and main devices, the current through the auxiliary switch and voltage across the auxiliary switch are shown in Fig. 3.14. These waveforms show the soft-switching of the auxiliary device. The waveforms of gating pulses, i_{Cr2}, v_{Link} for both cases of simulation and experiment are shown in Fig. 3.15.

The voltage across the main switch is the complement of the link voltage. As far as the soft-switching of the main switch is concerned, the soft-switching process is assisted by the auxiliary switch during turn-on and by the snubber capacitor across it during its turn-off. The phase current and the line-to-line voltage waveforms of the load under steady state are shown in Fig. 3.16. As mentioned above, all these waveforms shown in Figs. 3.14-3.16 correspond to the switching frequency of 25 kHz. At this switching frequency, the waveform of the phase current obtained under MSVM departs from sinusoidal as shown in Fig. 3.16.

In order to obtain improved current waveform, the switching frequency is increased. This is achieved by using an EPROM-based complete hardware circuit replacing the earlier data acquisition card which has frequency limitation. The complete hardware setup is fabricated using EPROM as shown in Fig. 3.8. The switching frequency of dc link switch is increased to about 38.5 kHz (sampling time $T_s = 26$ μs). Further, it is observed that the quality of phase current has improved due to reasonably high switching frequency. The simulation and experimental waveforms of the phase current and line-to-line voltage under steady state are shown in Fig. 3.17. For the sake of comparison, the harmonic analysis of the phase current by simulation for the reported soft-switching technique [36] and the proposed soft-switching technique is shown in Fig. 3.18 for the same load, modulation index and switching frequency. In the proposed technique, the fundamental component has increased and the harmonic amplitudes (5^{th} and 7^{th}) are reduced. The simulation and experimental results of current harmonics depicting amplitudes up to ninth including fundamental component for the proposed scheme are shown in Fig. 3.19. The measurements from the experimental setup show output current THD of 10 % and efficiency of 90%, while the respective values in simulation studies are found to be 8 % and 94%.

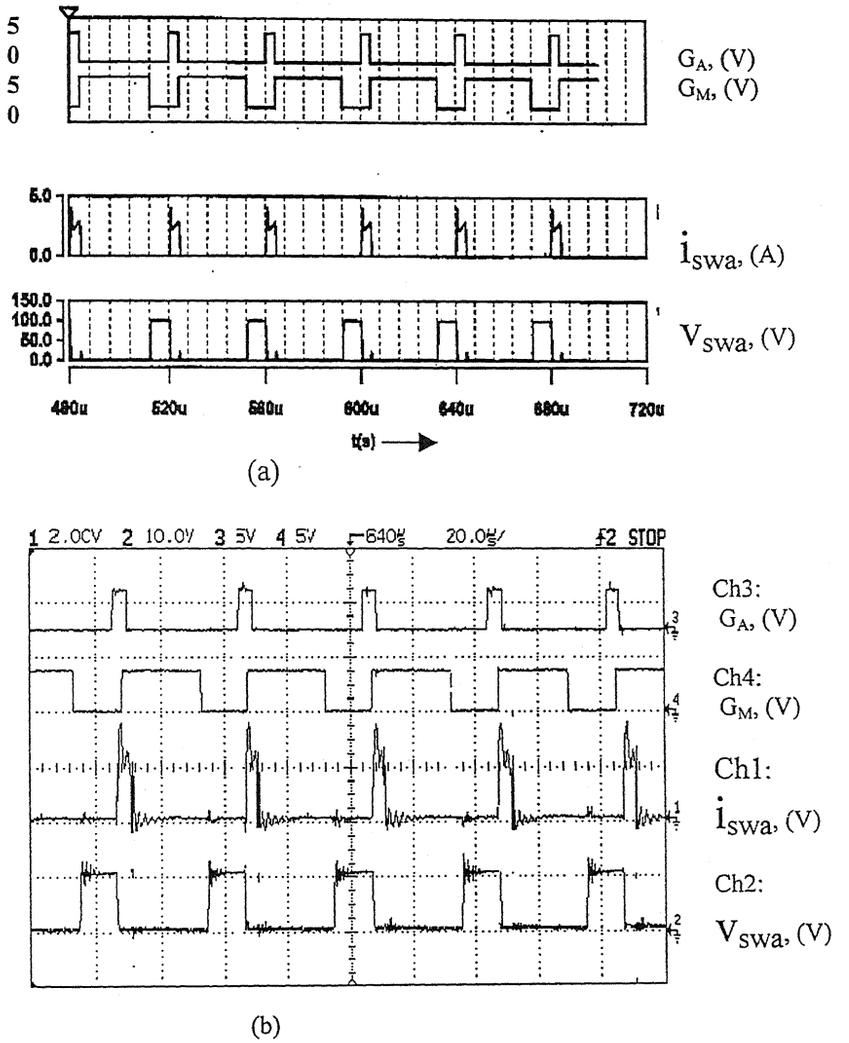


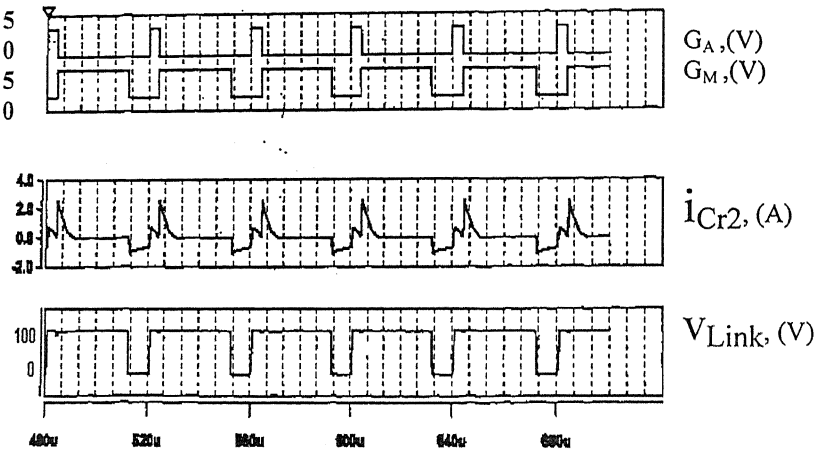
Fig. 3.14. Current (i_{swa}) through and voltage across (v_{aux}) the auxiliary switch obtained from SABER simulator and experimental setup.

G_A: Gate pulses of auxiliary switch (SW_A)

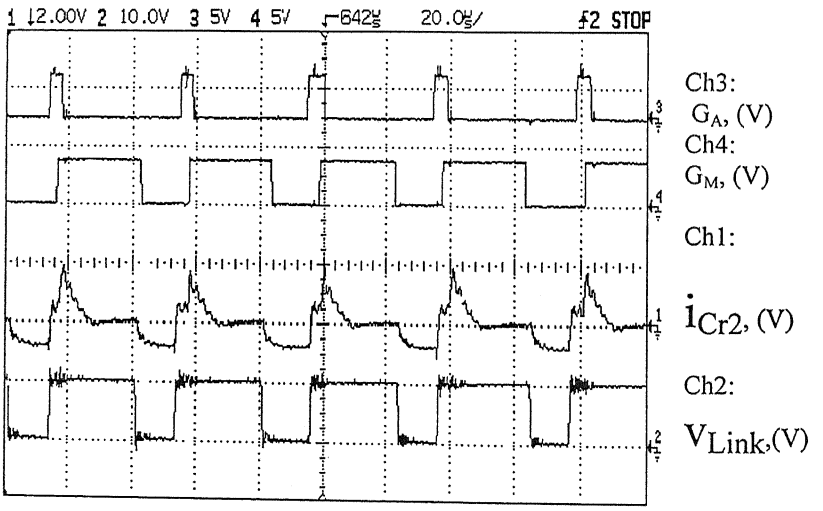
G_M: Gate pulses of main switch (SW_M)

(a) Simulation results

(b) Experimental results (scale for i_{swa}: 2Amp/volt, V_{swa}: 1:10)



(a)



(b)

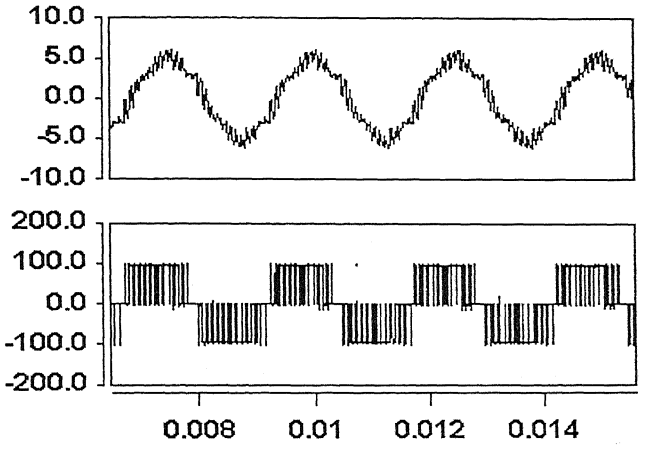
Fig. 3.15. Capacitor current (i_{Cr2}) and link voltage (v_{Link}) obtained from SABER simulator and experimental setup.

G_A : Gate pulses of auxiliary switch (SW_A)

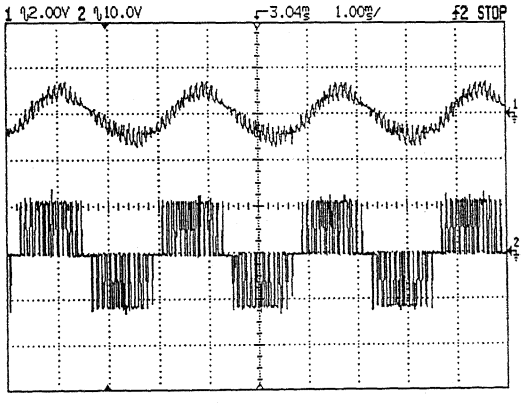
G_M : Gate pulses of main switch (SW_M)

(a) Simulation results

(b) Experimental results (scale -:i_{Cr2}: 2 Amp/volt, V_{Link}: 1:10)



(a)



(b)

Fig. 3.16. Phase current (i_a) and line-to-line voltage (V_{ab}) obtained from SABER simulator and experimental setup at switching frequency of 25 kHz

(a) Simulation results

(b) Experimental results: (scale- i_a : 2 Amp/volt, V_{ab}- 1:10)

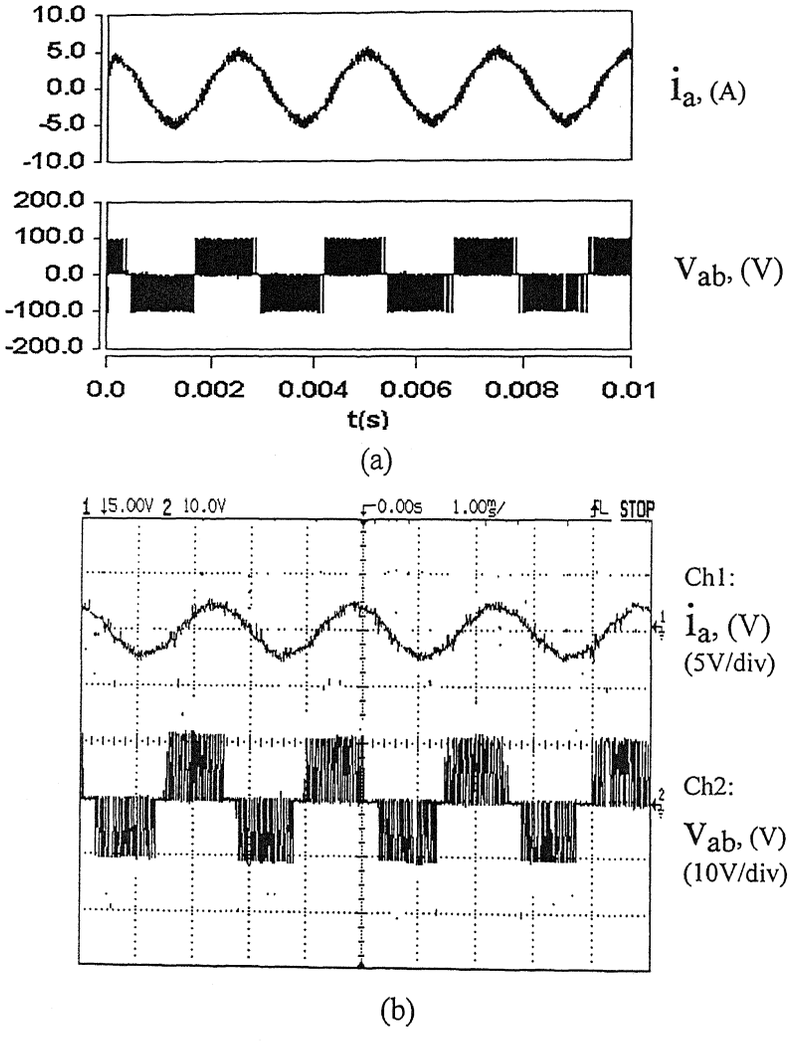


Fig. 3.17. Phase current (i_a) and line-to-line voltage (V_{ab}) obtained from SABER simulator and experimental setup at switching frequency of 38.5 kHz. (R_{Load} =10 Ω, L_{Load} = 400 μH)

(a) Simulation results

(b) Experimental results

Scale for

phase current : 2 Amp/volt

line-to-line voltage: 1:10

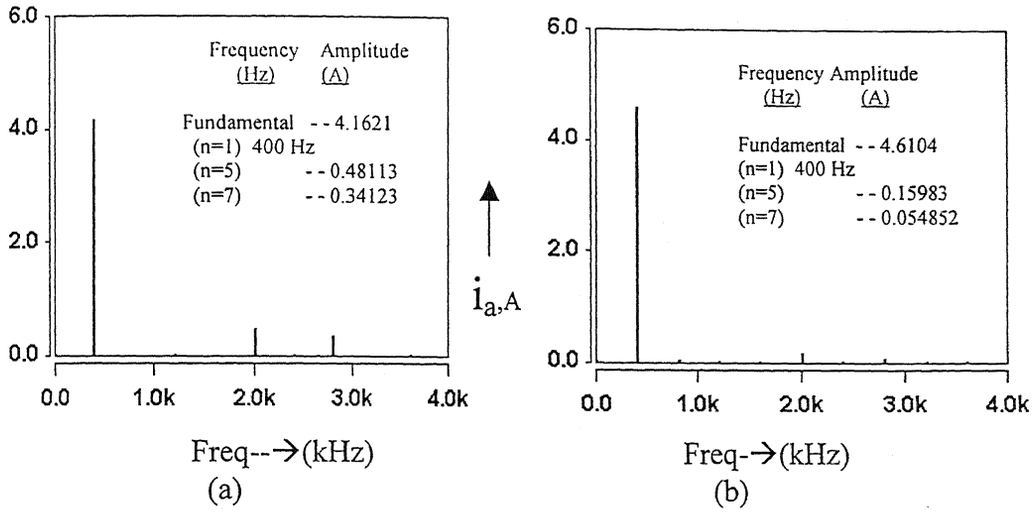


Fig. 3.18. Harmonic analysis of phase current for soft-switched SVM from simulation (R_{Load} = 10Ω, L_{Load} = 400 μH, dc link switching freq = 38.5 kHz, Modulation index = 0.75)
(a) Reported technique [3] (b) Proposed technique

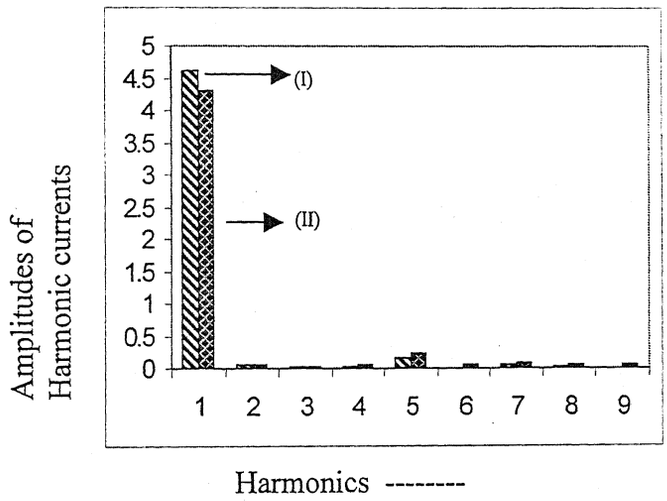


Fig.3.19. Harmonic analysis of phase current (i_a) obtained from proposed technique.
(I) Simulation result
(II) Experimental result

3.8 Conclusion

The two-switch quasi-resonant dc link (QRDCL) topology proposed in this chapter has made it possible to achieve ZVS and ZCS operation for both main and auxiliary switches in the quasi resonant dc link. An additional capacitor of low voltage rating and high capacitance has permitted the realization of ZVS for the auxiliary switch in the QRDCL. Besides, the inverter devices are also switched under ZVS after the link voltage is periodically made zero. Since the switching losses are considerably reduced due to ZVS and ZCS, the inverter is operated at a high frequency. This is highly desirable for inverters used in aerospace applications where space and weight are of paramount importance. There is a good agreement between simulation and experimental waveforms showing soft-switching of devices. A new technique of SVM called MSVM for soft-switched quasi-resonant dc link inverter has been analyzed by SABER simulator and verified experimentally. This technique is quite suitable over a wide range of frequency because of better volt-ampere utilization in each phase. Further, it requires less number of components for hardware implementation and a simple software program when compared to the conventional SVM technique. Another important feature is that the zero vectors in the new technique are implemented in a simple way than in the conventional SVM technique [39].

The present topology can be used for load of high power factor ($\geq$0.9). When the load power factor decreases, the current in the dc link becomes negative for certain duration and hence the dc link voltage cannot be brought down to zero by opening the main switch. As a result, soft-switching of inverter devices is not possible. Thus, there is a need for modification of the present topology when the power factor falls below typically 0.9. This is discussed in Chapter 4.

CHAPTER 4

A Novel Quasi-Resonant Inverter for Low and High Power Factor Loads

4.1 Introduction

The topology of quasi-resonant dc link inverter presented in Chapter 3 can handle loads of high power factor greater than or equal to 0.9. The dc link current for this condition is positive. However, depending upon the inverter frequency and load power factor, the link current may become negative for some duration. For instance, negative dc link current appears in an inverter for highly inductive or regenerative loads. With the negative link current, it may not be possible to make the link voltage zero even when both main and auxiliary switches are turned off. Consequently, ZVS operation is not possible for the above-mentioned topology during turn-on and turn-off for the switching devices of the inverter. To realize ZVS operation of power semiconductor switches in an inverter having negative dc link current, it is essential that the dc link voltage be made zero with some additional circuit configuration.

Various topologies of quasi-resonant inverters were proposed for both passive and active loads of lagging power factor [27-29], [31-32], [43-45]. A zero voltage transition (ZVT) inverter is reported in [27], where an auxiliary inverter along with a three-phase diode bridge is connected in parallel to the main inverter. Also, there exists a coupled inductor and a saturable core reactor between respective individual phases of the main inverter and the auxiliary inverter. The main inverter devices turn on/off under ZVS and the switching devices of the auxiliary inverter turn on/off under ZCS. Thus, six switches, twelve diodes, three coupled inductors and three saturable core reactors were used to achieve soft-switching for the switching devices of the main inverter. The topologies presented in [28, 29] were improved compared to the topology reported earlier in [27]. In these topologies an additional bridge inverter was used along with resonant components in each phase apart from the main inverter. To achieve soft-switching operation, it requires six additional switching devices, six diodes and three pairs of resonant

components for ZCS turn-off and/or ZVS turn-on of the main inverter switching devices. A novel technique using the resonant snubber-based principle was investigated in [31, 32] for both passive and active loads. The circuit consists of a resonant switch, a diode, and a resonant inductor in each phase of the load. These additional components in each phase form a star-connected /delta-connected arrangement across the three-phase load circuit to realize soft-switching of inverter devices. The Quasi-resonant link comprising of two switches having a reasonably high inductance in series with the source was discussed in [43]. The converter was designed to handle a passive load having displacement factor equal to 0.88 lagging. Quasi-resonant link comprising of three switches followed by GTO-based three-phase inverter supplying an induction motor load was reported in [44]. The inverter was operated at 2 kHz with the dc link at 60V. A soft-switching current controlled inverter capable of imposing good sinusoidal current waveform to an induction machine was reported in [45]. This circuit was operated at fairly high switching frequency using bang-bang current control strategy for the three-phase inverter. It was mentioned that one of the switches of the resonant link and all switches of the inverter turn on 'hard' and turn off 'soft'.

In this chapter, a novel topology is proposed for both passive and active loads operating at low and high power factor. To start with, effect of load power factor on the dc link current is explained with the help of a six-step inverter. The novel topology of QRDCL inverter is implemented with modified space vector modulation (MSVM) incorporating soft-switching operation. The design of resonant circuit parameters is given. The control strategy for the operation of the inverter is briefly presented. The complete quasi-resonant link three-phase inverter-load is simulated using SABER. A laboratory-sized model has been built and experimentally tested. Typical experimental results are provided to verify the validity of the simulation results.

4.2 Effect of Load Power Factor on the DC Link Current

In order to explain the case of positive and negative link current in an inverter, a six-step VSI is considered. In a normal six-step VSI, there are six switchings in a cycle represented by six vectors (V_1 - V_6) as shown in Fig. 3.5. Three switches conduct at any instant. Out of these three

switches, two switches conduct continuously in a sector and the third switch undergoes switching transition once at the beginning of each sector. This switching transition normally takes place between the devices in the same leg. Referring to Fig. 3.5 of Chapter 3 and assuming that the inverter is operating in Sector-I, the switching transition takes place between vectors V_1 and V_2. The switches S_{ap}, S_{bn}, and S_{cn} represent vector V_1 where as the switches S_{ap}, S_{bp}, and S_{cn} represent vector V_2. Thus, the two devices that are continuously biased in sector-I are S_{ap} and S_{cn} while switching transition takes place between the two devices S_{bp} and S_{bn} in the same leg. In case of a six-step VSI, the link current at any instant remains positive as long as the load power factor angle becomes less than or equal to 60^0 which is equal to one sector interval. As the load power factor angle exceeds 60^0, the link current becomes negative at the beginning of a sector and continues to be negative for a small interval. Thus, the time duration of the negative current within a sector depends on the fundamental frequency and values of load parameters.

The difference between the conduction of devices in an inverter when the load power factor angle is less than or equal to 60^0 and more than 60^0, has been shown here for Sector-I. Figure 4.1 shows the conduction of the switching devices for power factor angle less than or equal to 60^0, whereas Fig. 4.2 shows the same for load power factor angle more than 60^0. In both cases, the switches S_{ap}, S_{bn}, and S_{cn} representing vector V_1 remain on before the beginning of the sector. The switch S_{bn} is turned off and the switch S_{bp} is turned on at the end of sector-I. The earlier continuously conducting switches together with the incoming switch S_{bp} now represent vector V_2 at the beginning of sector-II

In Fig. 4.1(a), it is obvious that the dc link current is positive and the switching transition takes place in Fig. 4.1(b) from switch S_{bn} to S_{bp}. This can readily be seen as shown below.

On applying Kirchoff's current law at the node "X" of Fig. 4.1(b),

$i_a = i_{Link} + i_b$.

As $i_a = i_b + i_c$ and $i_a > i_b$, so the link current $i_{Link} = (i_a - i_b)$ is positive.

In Fig. 4.2(a), though the switching devices S_{ap}, S_{bn}, and S_{cn} are biased similar to Fig. 4.1(a), the switch S_{cn} is not turned on as the anti-parallel diode D_{cn} is forward-biased. Therefore the devices S_{ap}, S_{bn}, and the diode D_{cn} across the switch S_{cn} conduct. Such a situation arises with low power factor load. The current equation is $i_b = i_a + i_c$ under balanced condition and the dc

link current is positive and equal to phase-a current. When the switching transition takes place from the switch S_{bn} to the switch S_{bp} as shown in Fig. 4.2(b), the device S_{bp} does not conduct, but it is the diode D_{bp} across the switch S_{bp} that conducts. This can easily be seen by KCL at the node "X" as follows.

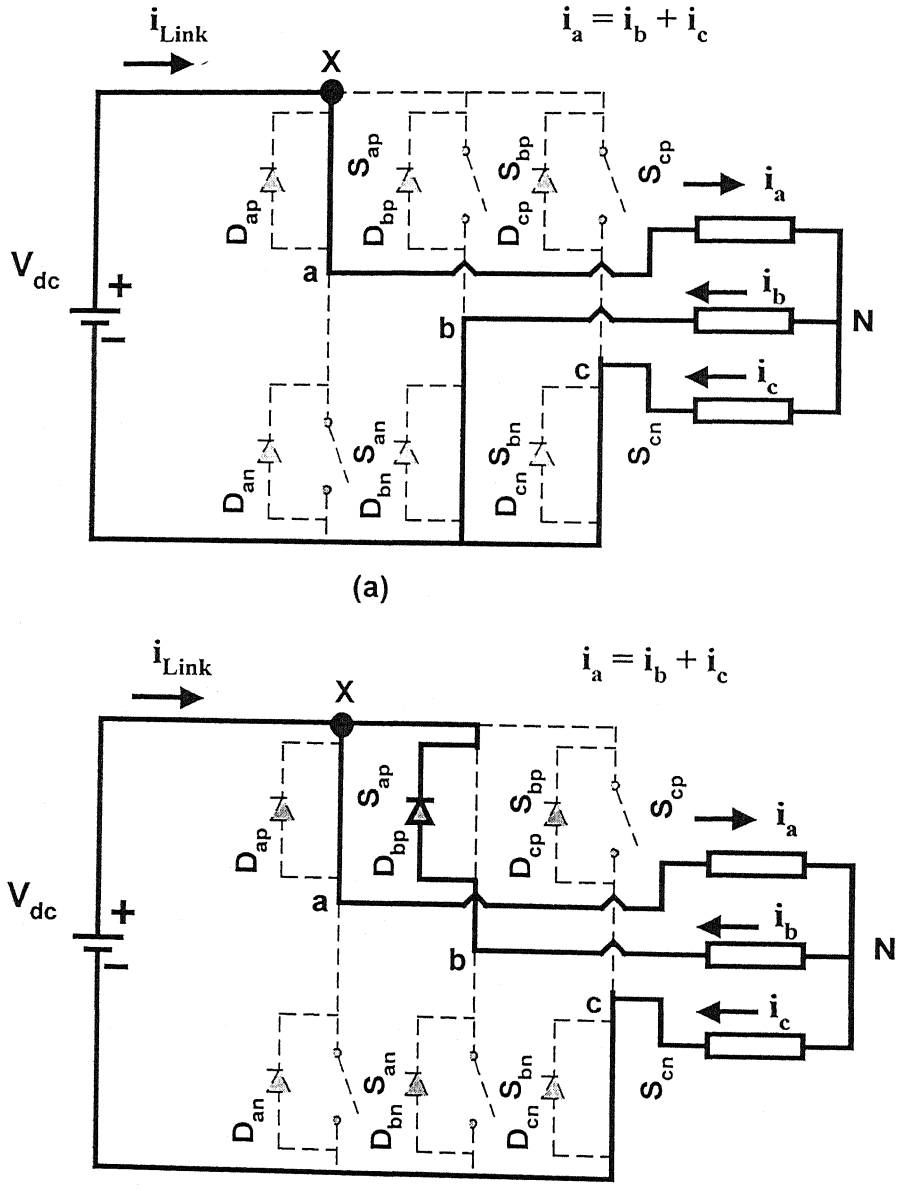


Fig. 4.1: Conduction of switching devices in a sector during high power factor load. (phase angle $\leq 60^0$)
(a) before switching transition
(b) after switching transition (i.e., from switch S_{bn} to S_{bp})

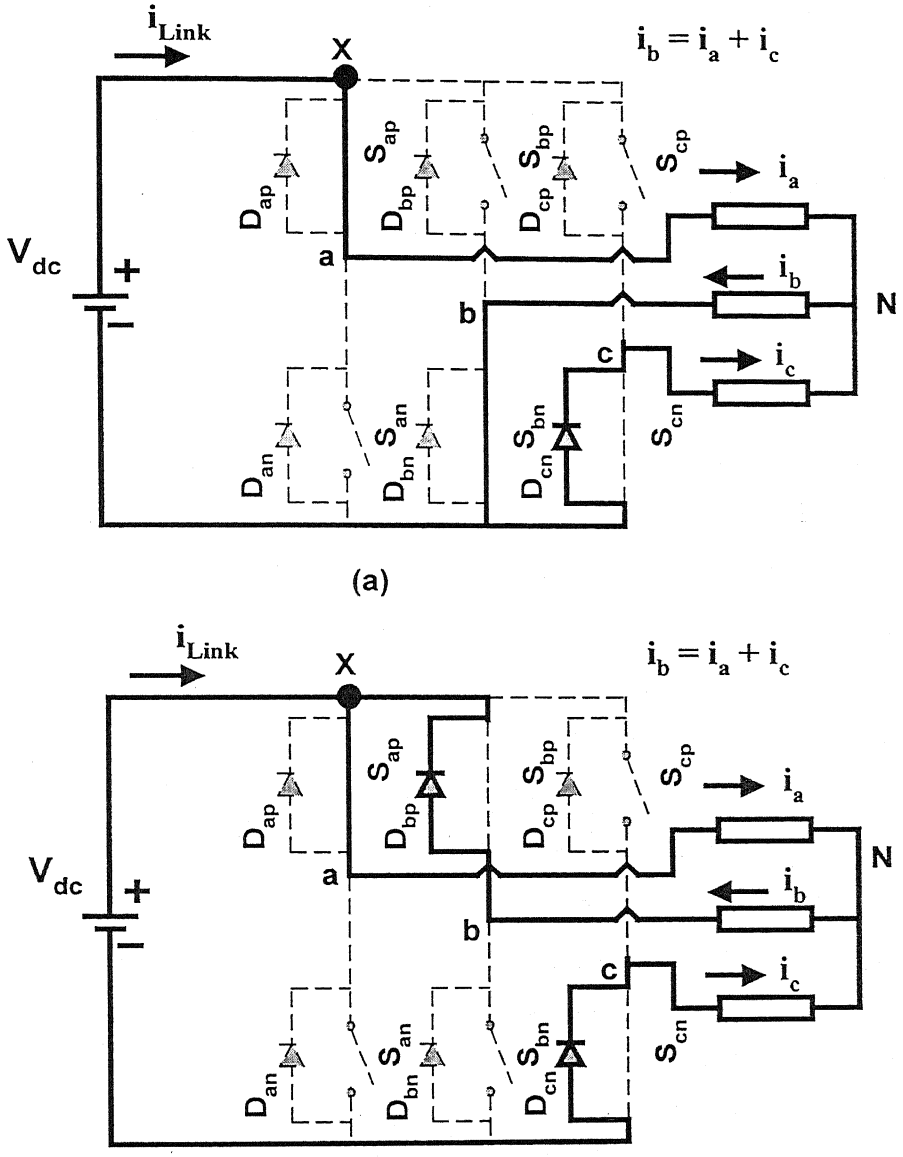


Fig. 4.2: Conduction of switching devices in a sector load during low power factor load. (Phase angle > 60^0)

(a) before switching transition

(b) after switching transition (i.e., from switch S_{bn} to S_{bp})

$i_a = i_{Link} + i_b$.

As $i_b > i_a$, the link current ($i_{Link} = i_a - i_b$) is negative. This negative current will persist in the dc link during every switching from the switch S_{bn} to S_{bp} as long as the diode D_{bp} remains forward-biased.

From the above discussion it follows that the current changes its direction in dc link during transition of switching devices under different load power factor angles.

4.3 Proposed Topology and Modes of Operation

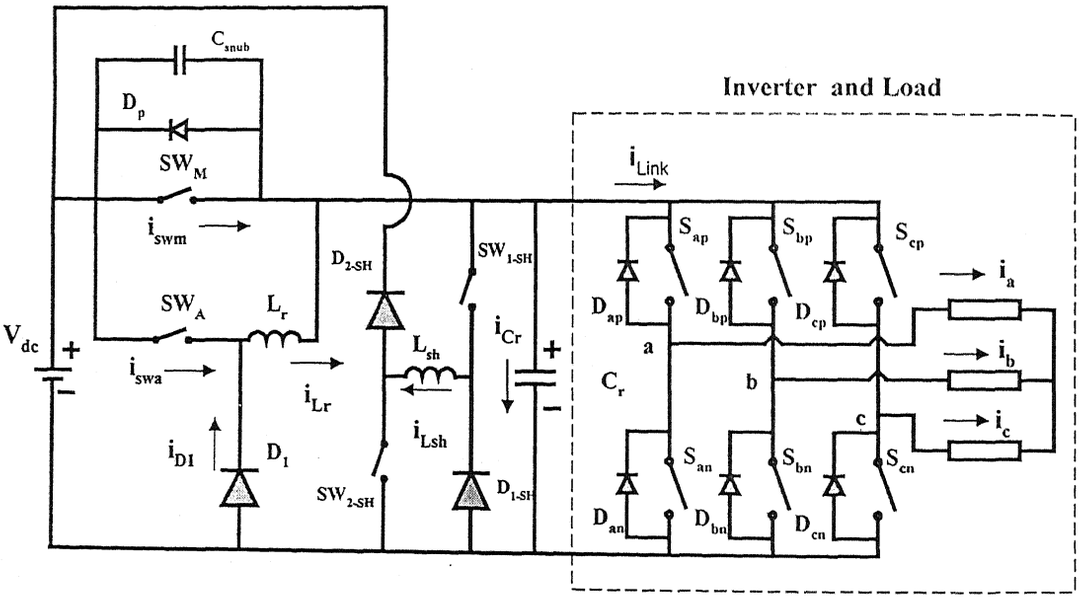


Fig. 4.3: The proposed topology for low and high power factor load

The proposed quasi-resonant dc link topology is shown in Fig. 4.3 with ripple-free dc link current. The dc link current is designated as positive when flowing from the source to the inverter, and as negative when it is vice versa. The topologies in [41, 42] provide soft-switching operation when the link current is positive but they fail to provide the same when the link current of the inverter is negative under low power factor condition. The topology of Fig.4.3 has the ability to provide zero-voltage switching (ZVS) for all inverter switches for both positive and

negative link current i_{Link}. This happens when the load power factor is low. The soft-switching of inverter devices during positive and negative dc link current is explained separately.

CASE-A: ***When the link current is positive.***

The circuit diagram of Fig. 4.4(a), marked with solid lines shows the state of the topology of Fig. 4.3 as the initial condition. In this state, the main switch SW_M conducts the load current and the resonant capacitor across the link is clamped to the source voltage. No other devices conduct in the resonant link. During soft-switching of inverter devices, the circuit of Fig. 4.4(a) goes through various modes of operation as shown in Fig. 4.4(b-e). The corresponding switching waveforms during these modes of operation are shown in Fig. 4.5.

Mode-I ($t_0 - t_1$): Mode-I (Fig. 4.4(b)) is initiated with withdrawal of gate signal from switch SW_M at t_0 as shown in Fig. 4.5. The resonant capacitor discharges to zero voltage within a small interval of the duration of this mode. The anti-parallel feedback diodes across the inverter switches get forward-biased because of zero voltage. The inverter switching status is changed at this instant under ZVS. This mode ends at t_1 when the gate pulse to the auxiliary switch is released.

Mode-II (t_1 - t_2): The mode starts with the turn-on of auxiliary switch SW_A as shown in Fig. 4.4(c). The current through the resonant inductor L_r increases linearly from zero, while the current through the feedback diodes in the inverter decreases. The auxiliary switch is turned on under ZCS because of series inductor L_r. This mode ends when the current through the resonant inductor (L_r) is equal to link current and the current through the feedback diodes becomes zero.

Mode-III (t_2 - t_3): Mode-III starts with the charging of capacitor C_r due to resonance between L_r and C_r, and the circuit topology is as shown in Fig. 4.4(d). The inductor current is equal to the sum of charging current of capacitor C_r and the link current, i_{Link}. The voltage across the dc link gradually builds up from zero to the voltage equal to the source voltage. Further increase in the link voltage due to resonance of L_r and C_r causes the diode D_p to be forward-biased. When the link voltage becomes equal to the source voltage, the auxiliary switch SW_A is turned off and the main switch SW_M is turned on. Thus, the mode ends at t_3 as shown in Fig. 4.5.

Mode-IV (t_3-t_4): During this mode (Fig. 4.4(e)) the auxiliary switch SW_A is turned off and the main switch SW_M is turned on at t_3. The resonant inductor current is more than the link

current. The excess current over the link current flows through the anti-parallel diode D_p. This mode ends when the inductor current becomes equal to the load current.

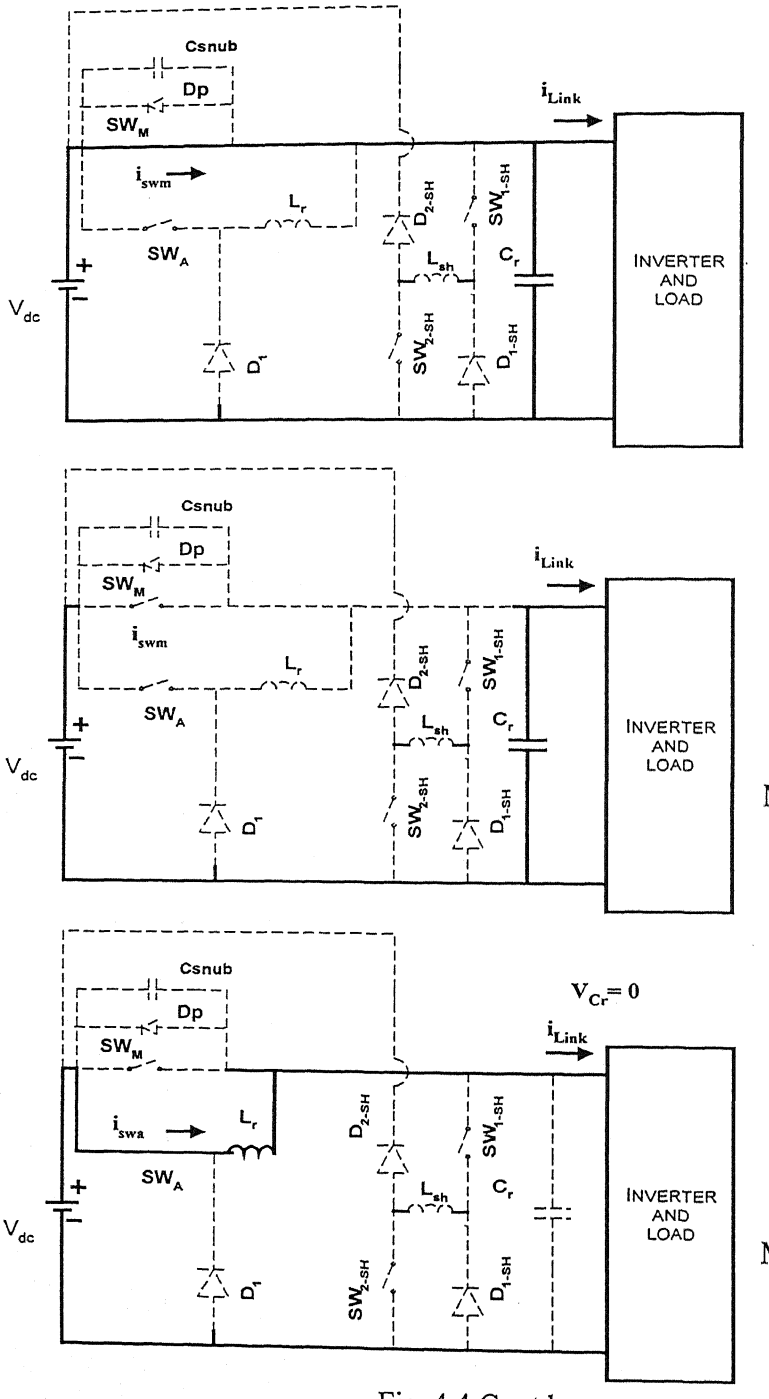


Fig. 4.4 Contd.

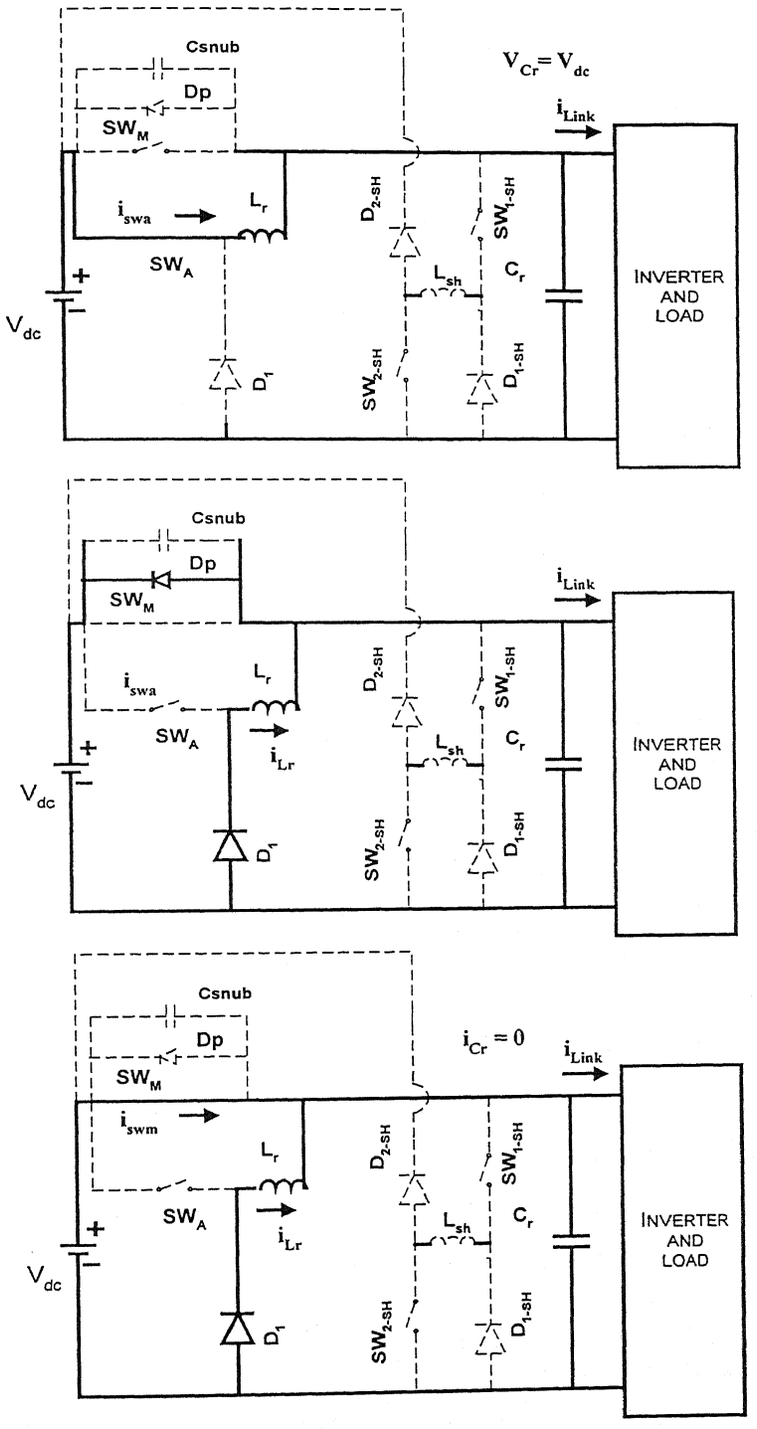


Fig. 4.4: Modes with positive dc link current

Mode-V (t_4-t_5): Mode V (Fig. 4.4(f)) starts with the turn off of the diode D_p at t_4 and at the same time, the main switch starts conducting. The link current is now the sum of the resonant inductor current and the main switch current. This mode ends at t_5 when all the energy stored in the resonant inductor is recovered and the main switch conducts the total link current. The circuit topology changes to the initial status of Fig. 4.4(a) and the same modes repeat.

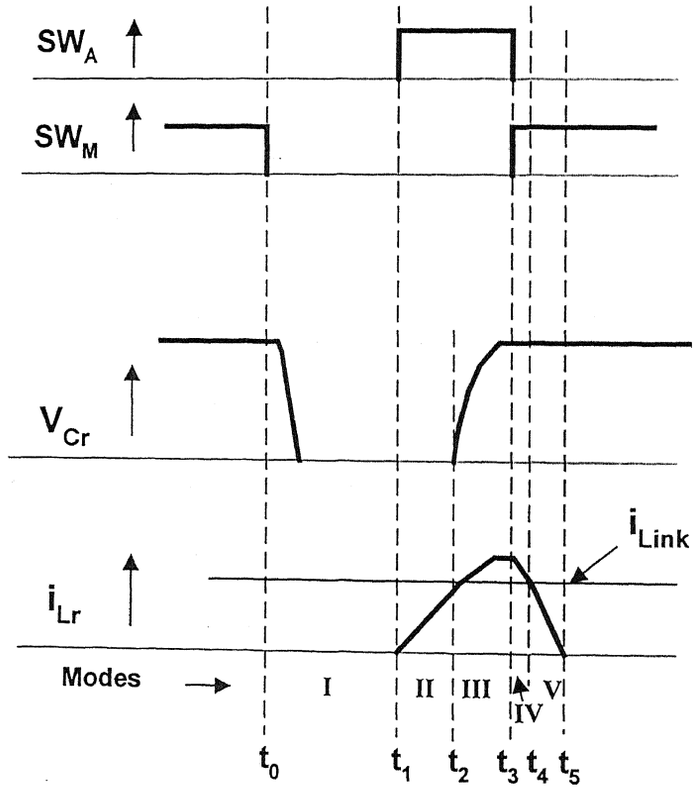


Fig. 4.5 Switching waveforms under positive dc link current

CASE-B: ***When the link current is negative***

The initial circuit topology is shown in Fig. 4.6(a). The link current is assumed to be negative. The dc link/capacitor voltage is clamped to the source voltage due to conduction of

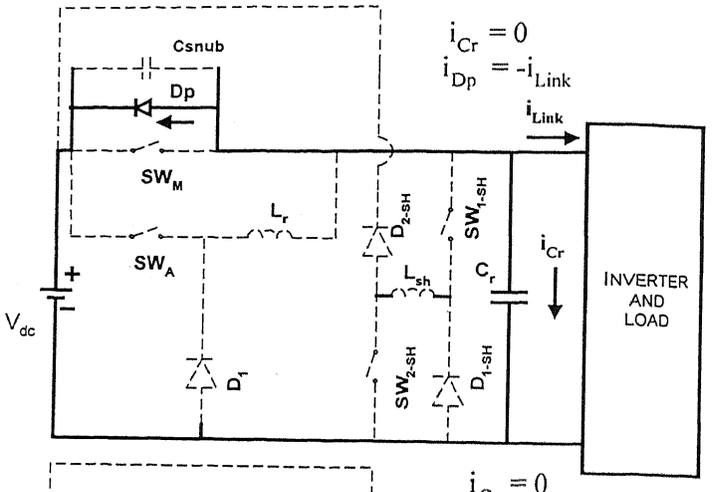
diode D_p. The diode D_p conducts the negative dc link current. All the switching devices in the resonant link are in the off state. The following modes show how the switching status of the inverter is changed during negative dc link current. The waveforms of gating signals to shunt switches, resonant capacitor voltage, and the shunt inductor current during various modes of operation are shown in Fig. 4.7.

Mode-I (t_0-t_1): Mode-I (Fig. 4.6(b)) starts with releasing of gating pulses to shunt-switches ($SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$) at t_0 as shown in Fig. 4.7. The link voltage still remains clamped to the source voltage because of conduction of diode D_p. The current in L_{sh} increases linearly from zero. The negative dc link current is the sum of currents in diode D_p and inductor L_{sh}. This mode ends when the inductor current i_{Lsh} becomes equal to the load current. The diode D_p becomes reverse-biased and turns off.

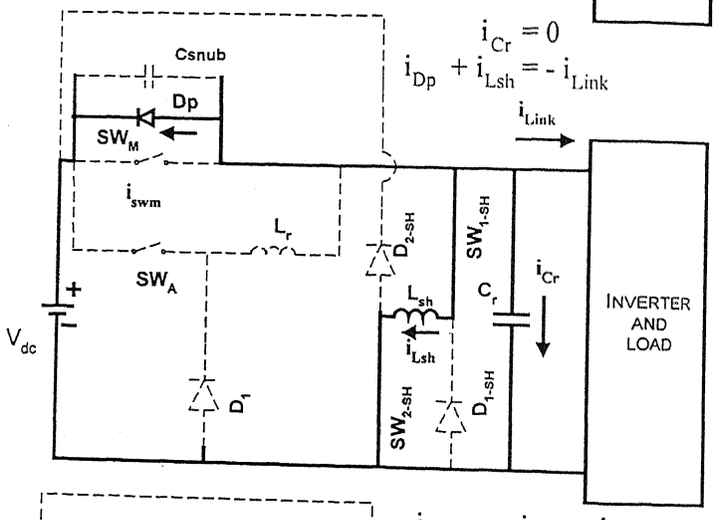
Mode-II (t_1-t_2): When the diode D_p turns off, the resonant capacitor starts discharging. The mode begins at t_1 as shown in Fig. 4.6(c). The current in L_{sh} is the sum of negative dc link current and discharging capacitor current. This mode ends when the capacitor C_r discharges to zero voltage.

Mode-III (t_2-t_3): When the resonant capacitor discharges to zero voltage, the switching status of inverter devices is changed under ZVS. The circuit topology valid for mode-III is shown in Fig. 4.6(d). At this instant, due to energy in the resonant inductor L_{sh}, the diode $D_{1\text{-}SH}$ gets forward-biased through $SW_{2\text{-}SH}$. The dc link is shorted through $SW_{1\text{-}SH}$ and the forward-biased diode $D_{1\text{-}SH}$. The current through $D_{1\text{-}SH}$ is the difference between shunt inductor current and negative dc link current. The switch $SW_{2\text{-}SH}$ conducts the shunt inductor current. This mode ends with the withdrawal of gating pulses from shunt-switches $SW_{1\text{-}SH}$ and $SW_{2\text{-}SH}$.

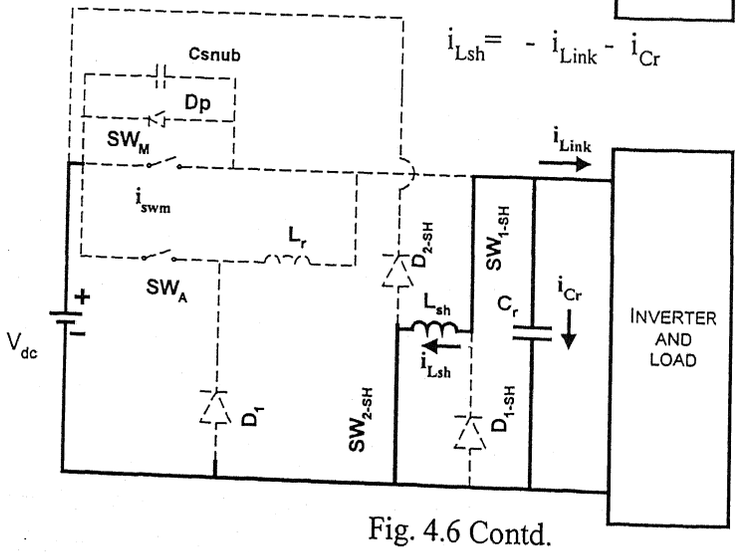
Mode-IV (t_3-t_4): With the withdrawal of gating pulses from shunt-switches at t_3, the energy in inductor L_{sh} is recovered to the source through diodes $D_{1\text{-}SH}$ and $D_{2\text{-}SH}$. This mode starts with conduction of diodes $D_{1\text{-}SH}$ and $D_{2\text{-}SH}$ as shown in Fig. 4.6(e). The current in the inductor decays to zero. Simultaneously, the capacitor is charged with constant negative dc link current and the mode ends when the capacitor voltage becomes equal to the source voltage. The diode D_p becomes forward-biased and conducts full-load current. The shunt-switches turn off under ZVS. Now the circuit topology changes to initial circuit of Fig. 4.6(a) when the next cycle of operation is initiated.



(a)



(b)
Mode-I



(c)
Mode-II

Fig. 4.6 Contd.

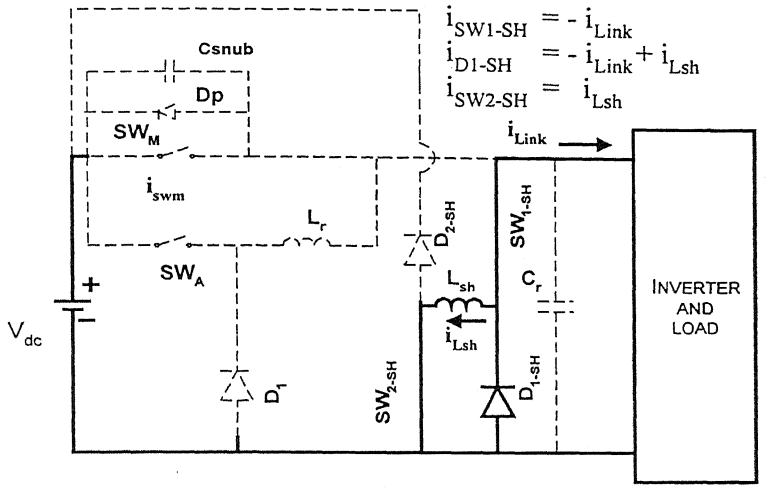


Fig. 4.6: Modes with negative dc link current

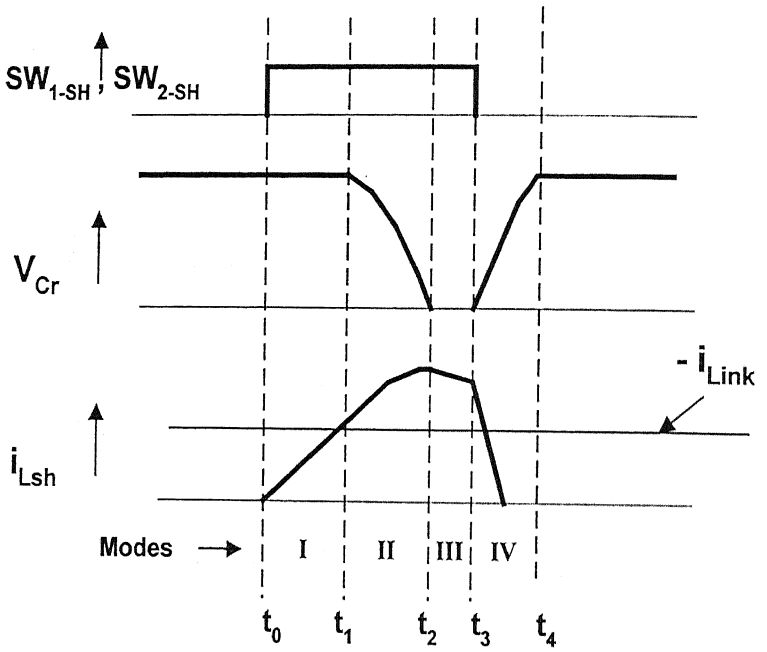


Fig. 4.7. Switching waveforms with negative dc link current

CASE-C: *When the link current is partly positive and partly negative*

The dc link current depends upon load voltage and its power factor. The waveform of the dc link current repeats after each interval of sector. The duration of each sector is one-sixth of the fundamental period at output frequency. In the case of loads of high power factor, the link current is unidirectional from the source to the load. On the other hand, with power flow from source to inverter supplying loads of low power factor, the dc link current is partly negative and partly positive in each sector. In case of regenerative operation, the situation prevails for the dc link current with power flow from the inverter-load to the source. However, the intervals of positive and negative dc link current during each sector are interchanged. Therefore, it is desirable to develop a quasi-resonant inverter topology which permits soft-switching of inverter devices independent of the direction of dc link current. In this section, the schemes described earlier are combined so that the control strategy provides soft-switching independent of the direction of the dc link current. In order to make the circuit operation simple and independent of

the direction of the dc link current, the operation of shunt-switches described in Case-B is combined with the operation of Case-A. As a result, the following steps of operation are brought out and built into the control circuit. The sequence of operation is performed every time to implement ZVS operation of inverter switches whenever a change in the switching status of inverter devices is needed.

Step-I: Gate pulses to both main and auxiliary switches SW_A and SW_M are withdrawn.

Step-II: Shunt switches, $SW_{1\text{-}SH}$ and $SW_{2\text{-}SH}$ are turned on by releasing gate pulses.

Step-III: The status of inverter switches is changed after the resonant capacitor C_r discharges to zero.

Step-IV: The shunt switches ($SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$) are turned off.

Step-V: The auxiliary switch is turned on for a small interval.

Step-VI: As the dc link attains the source voltage, the main switch is turned on while the auxiliary switch SW_A is turned off.

The switching waveforms of gating pulses of all resonant link switches, resonant capacitor voltage and resonant inductor current incorporating steps-I to VI are shown in Fig. 4.8. The gating pulses for the link switches shown in Fig. 4.8(a) allow soft-switching of inverter devices for both negative and positive dc link current. The waveforms of resonant capacitor voltage and resonant inductor current shown in Fig. 4.8(b) correspond to the case when the link current is positive, while the waveforms of resonant capacitor voltage and the resonant shunt inductor current shown in Fig. 4.8(c) correspond to the case when the link current is negative.

Step I is initiated with the removal of gating pulse to the main switch at t_o. In case of negative dc link current, the diode D_p conducts and the link voltage is clamped to the source voltage. On the other hand, if the link current is positive, the resonant capacitor across the dc link discharges to zero through the inverter and load. Step II is initiated at t_1 with the turn-on of shunt switches $SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$. In case of negative link current the dc link voltage continues to be clamped at the source voltage due to conduction of the diode D_P. The current through the shunt inductor

increases linearly from zero to the dc link current while the current through D_P turns off at t_2. From t_2 onwards, the link voltage is no longer clamped to the source voltage due to reverse biased diode D_P. The resonant capacitor starts discharging through the shunt inductor L_{Sh}. The shunt inductor current increases resonantly from its initial value of i_{Link}. The resonant capacitor discharges resonantly to zero at t_3. Step III is initiated with the soft-switching of inverter devices under ZVS at t_3. The diode $D_{1\text{-}SH}$ is forward biased by the trapped energy in L_{Sh} and conduction of shunt switch $SW_{2\text{-}SH}$. This continues until the removal of gating pulses from the shunt switches at t_4. In case of positive link current, the link voltage continues to remain at zero until the auxiliary switch is turned on. However, the switching status of inverter device is changed at t_3 as in the case of negative dc link current. This ensures that the link voltage is held at zero before switching of inverter devices is initiated for both positive and negative link currents. Step IV is initiated with the removal of gating pulses from shunt switches at t_4. The energy trapped in the shunt inductor is recovered to the source through conduction of diodes $D_{1\text{-}SH}$ and $D_{2\text{-}SH}$. The resonant capacitor is charged linearly by the negative dc link current and it continues until the link voltage becomes equal to the source voltage. Then the diode D_p gets forward biased and conducts the negative link current. Step V is initiated with the release of gating signal to the auxiliary switch SW_A. This does not have any effect when the link current is negative. In case of positive link current, the auxiliary switch turns on under ZCS due to resonant inductor L_r. The current through the resonant inductor increases linearly until it becomes equal to the link current at which the feedback diodes become reverse biased. At t_6, the excess current through the resonant inductor charges the link capacitor resonantly. This continues until the link voltage becomes equal to the source voltage. At this instant t_7, step VI is initiated by turning on SW_M and turning off SW_A. The excess current in the resonant inductor is fed back to the source through diode D_P. When the inductor current becomes equal to the link current, the diode D_P turns off. The main switch turns on under ZVS and supplies the load current along with the resonant inductor. As the resonant inductor current falls to zero, the main switch carries the link current. In case of negative link current, the operation of main and auxiliary switches does not have any effect. This explains the soft-switching operation when the link current is positive or negative and the dc link is now ready for the next soft-switching operation.

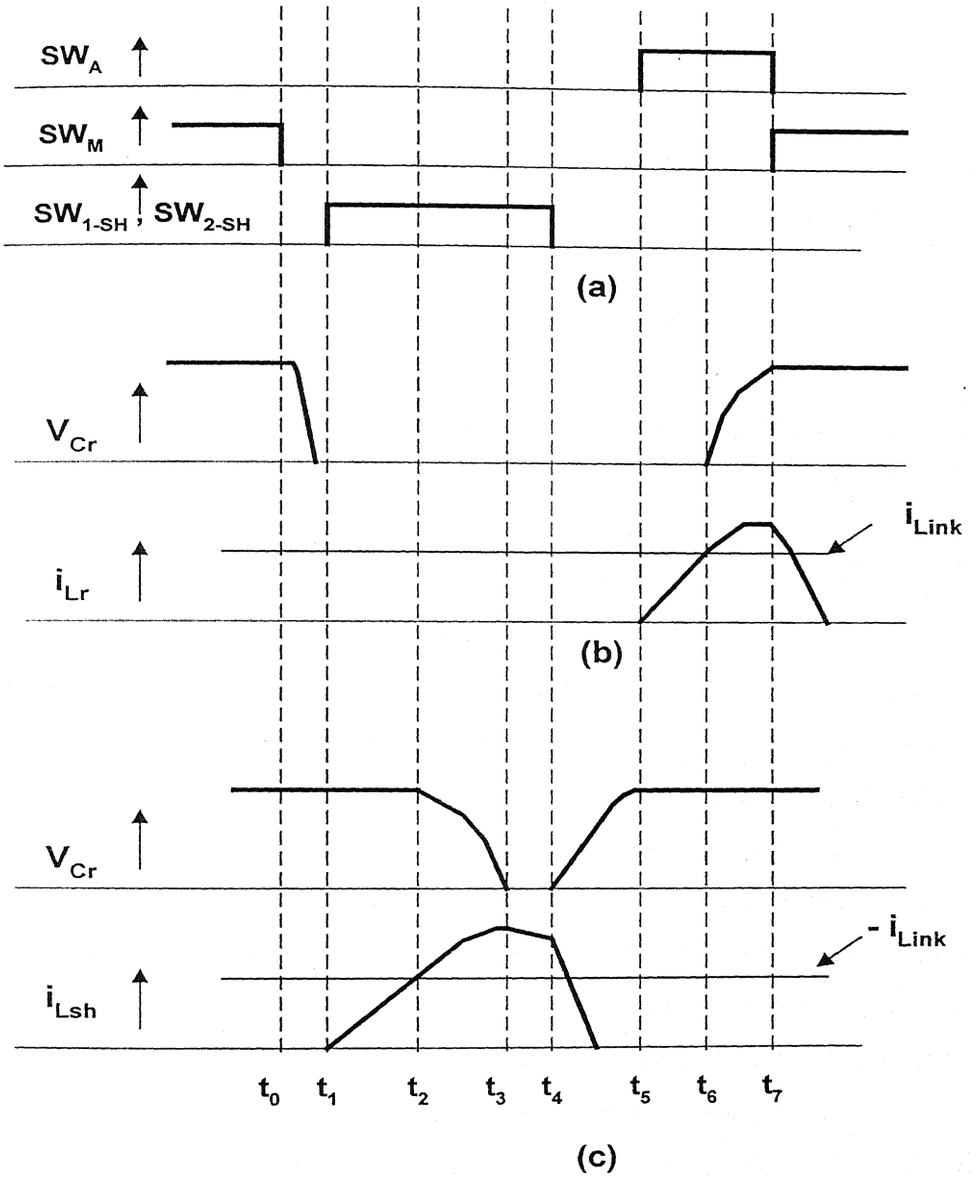


Fig. 4.8. Switching waveforms with positive and negative dc link current
(a) Gating pulses to dc link switches
(b) Waveforms of V_{Cr} and i_{Lr} when dc link current is positive
(c) Waveforms of V_{Cr} and i_{Lsh} when dc link current is negative

4.4 Control Strategy

The control strategy is similar to that described in Section (3.4) for the soft-switched MSVM. There is, however, some difference due to the introduction of shunt switches. Before the auxiliary switch is enabled, the shunt switches are supplied with gating pulses of small fixed duration. The initiation of soft-switching operation of inverter devices is enabled immediately after the turn-off of shunt switches.

In the soft-switching MSVM technique, the gating pulses for the switching devices in the resonant link and inverter for the case of Sector-I are shown in Fig. 4.9. The devices S_{ap} and S_{cn} are continuously on and soft-switching transition takes place between S_{bp} and S_{bn} similar to that described in Section 3.4. The calculations for the duration of zero vectors and non-zero vectors (t_1, t_2, t_{z1} and t_{z2}) are similar to those discussed in Section 3.4. The switching cycle is initiated with the closure of shunt switches ($SW_{1\text{-}SH}$ and $SW_{2\text{-}SH}$) under ZCS. Prior to this, the dc link main switch (SW_M) and the auxiliary switch (SW_A) are already turned-off. In case of positive link current from the source to the load, the dc link voltage across the inverter discharges to zero before the shunt switches are closed. If the link current is negative from the load to the source, there will be finite link voltage. In this case, it is necessary to close the shunt switches for discharging the resonant capacitor to zero voltage. The closure of the shunt switches helps to achieve ZVS operation independent of the direction of link current. Also, it makes the control technique simple, avoiding complexity in implementation. The shunt switches are closed for a small fixed interval within the zero vector period. The resonant capacitor voltage is discharged to zero without any need to monitor the direction of resonant link current. The shunt devices are then turned off. The switching status of inverter devices is changed. Soft-transition takes place from the switch S_{bp} to the switch S_{bn} of the inverter. The auxiliary switch is turned on for a fixed short duration before the end of zero-vector period. This turn-on pulse for the auxiliary switch is synchronized with the termination of the zero-vector period. The turn-off of the auxiliary switch and the turn-on of the main switch are also synchronized. The first non-zero vector is established for time duration of 't_1'. At the end of non-zero vector period (t_1), the first zero vector (V_{z1}) is realized with the opening of the main switch (SW_M) without any modification in switching status of the inverter. Before the zero vector duration (t_{z1}), the shunt switches are closed for a short

interval and then they are opened when the dc link voltage falls to zero. At this instant, the inverter device S_{BN} is turned off and S_{BP} is turned on under ZVS. Soon after this operation, the auxiliary device is turned on for a fixed duration. At the end of duration 't_{z1}', SW_A is turned off and SW_M is turned on to realize second non-zero vector (V_2). This non-zero vector (V_2) will continue for a period of t_2. At the end of this period of non-zero vector (t_2), the second zero vector (V_{z2}) is realized by opening the main switch without any change in switchings of inverter devices. The second zero vector continues for 't_{z2}'. Within the interval 't_{z2}' the shunt switches

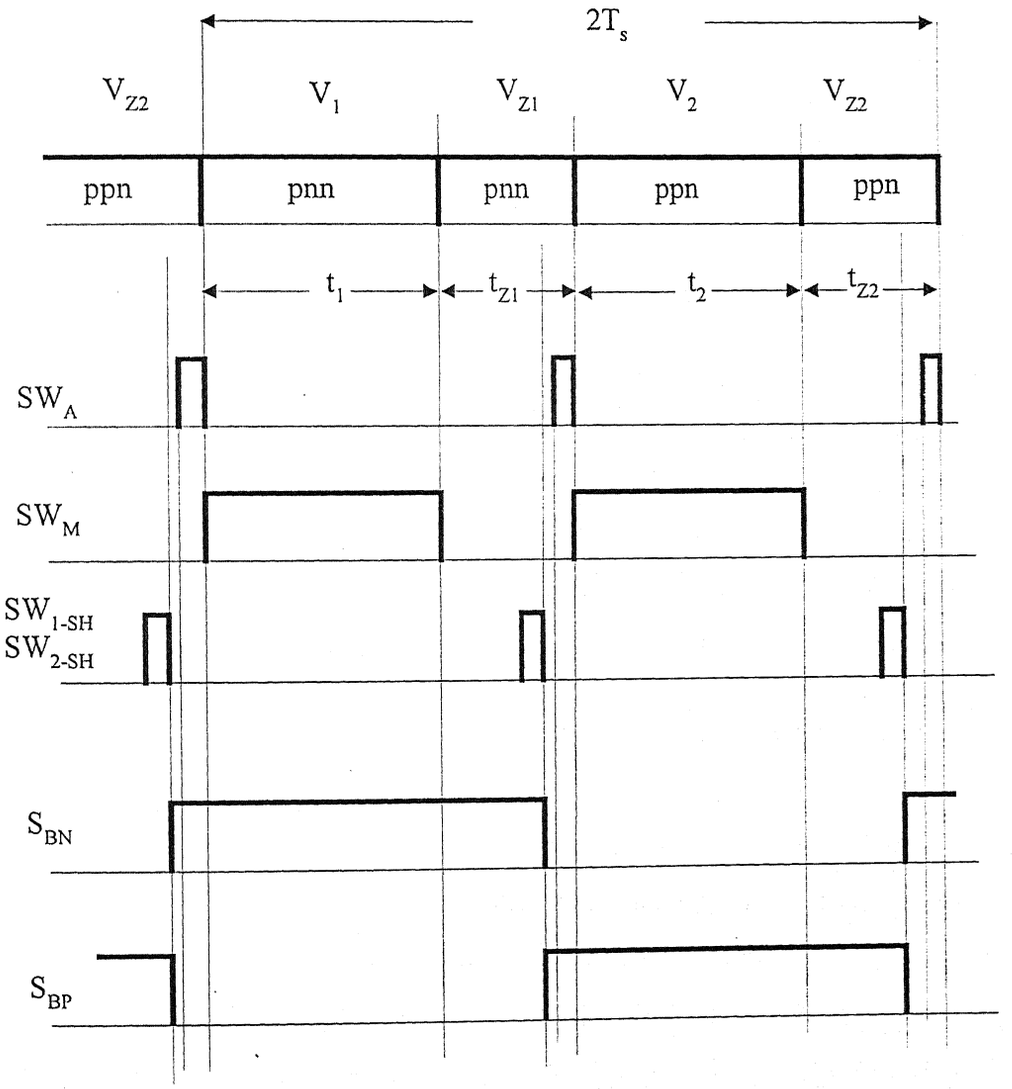


Fig. 4.9. Control technique of modified space vector modulation (MSVM)

($SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$) are closed. Thus, the switching process repeats for another switching cycle.

4.5 Design of Resonant Components

The design procedure for resonant components is more or less similar to that discussed in Section (3.3). In Section (3.3), there are two capacitors (Cr_1 and Cr_2) and one resonant inductor (L_r) in series with the auxiliary switches. In this case, there are two resonant inductors and one capacitor. Before designing the circuit components, the following data is required as explained in Section (3.3)

(a) Device critical (di/dt). This can be obtained from manufacturer's specification $(di/dt)_{cr}$.

(b) Load current (I_o)

(c) Source input voltage (V_{dc})

Step-1 (Lr): L_r is computed under the fact that circuit (di/dt) must be less than or equal to device critical (di/dt)

$$(di/dt)_{ckt} \leq (di/dt)_{cr} \qquad (4.1)$$

where $(di/dt)_{ckt} = V_{dc} / L_r$. Once $(di/dt)_{cr}$ is known, the value of L_r can be determined from (4.1).

Step-2 (C_r): C_r is computed using the condition that the resonant peak current through C_r must be less than or equal to the load current.

$$V_{dc} \sqrt{(C_r/L_r)} \leq I_0 \qquad (4.2)$$

where I_0 is the load current in case of dc output load or the input current to the inverter.

C_r is obtained from (4.2) when other parameters are known.

Step-3 (L_{sh}): L_{sh} is computed using the condition that when the shunt switches (SW_{1_SH}, SW_{2_SH}) are closed, the peak discharge current of the resonant capacitor through the shunt inductor (L_{sh}) must be greater than the load current. This condition is necessary to ensure that the link voltage discharges to zero in the first quarter of the resonant period ($2\pi\sqrt{(L_{sh} C_r)}$).

$$V_{dc} \sqrt{(C_r/L_{sh})} > I_0 \qquad (4.3)$$

The shunt inductor is designed such that it can discharge the resonant capacitor voltage to

zero as fast as possible. This helps in achieving ZVS operation of inverter devices immediately after the shunt switches are turned off.

4.6 Implementation

The novel QRDCL inverter is built using IGBT switches with driver cards. The switches are controlled by a personal computer (PC) through software. The driver card is designed and built for interface between personal computer (PC) and quasi-resonant three-phase inverter. It isolates the power circuit to control circuit using high-speed opto-isolator (IC 6N137). The details of the opto-isolator are given in Appendix-C. The block diagram for hardware implementation is shown in Fig. 4.10.

The desired signals for the switching devices in the resonant link inverter are derived from a data-acquisition card (ACL-8112 PG) connected to a PC having Pentium-III MMX CPU operating at a clock frequency of 450 MHz. The data-acquisition card has provision for 16-bit channels for analog-to-digital (ADC) conversion, two digital-to-analog (DAC) conversion channels, two 8-bit digital input /output port and a user-friendly independent timer counter fed with a 2 MHz clock. For implementation of the soft-switched MSVM scheme, one 8-bit digital output port and a timer counter are required. The availability of high-speed timer counter (8254), which is better than the conventional timer (8253), is programmed to operate in Mode-0 to derive pulse widths of different duration for the gate circuits of the inverter and link switches.

As seen from the control strategy discussed in the previous section, it needs a total of nine signals (one signal for the auxiliary switch, one signal for the main switch, one common signal for both shunt switches and six different signals for inverter switches) to be out from the data-acquisition card to interface with the hardware circuit. Usually, six signals are derived from the data-acquisition card out of which three signals are for the resonant link and the rest are for the inverter's upper half switches. These three signals for upper-half of the inverter switches are further inverted through the logical inverter circuits to connect to the lower half of inverter switches. The flow-chart as shown in Appendix-D is developed and the program is written using C++ compiler so as to load into a PC. The PC houses the data-acquisition card from which the desired signals are derived. These signals go through buffer and isolator stage before applying them to IGBT driver circuits.

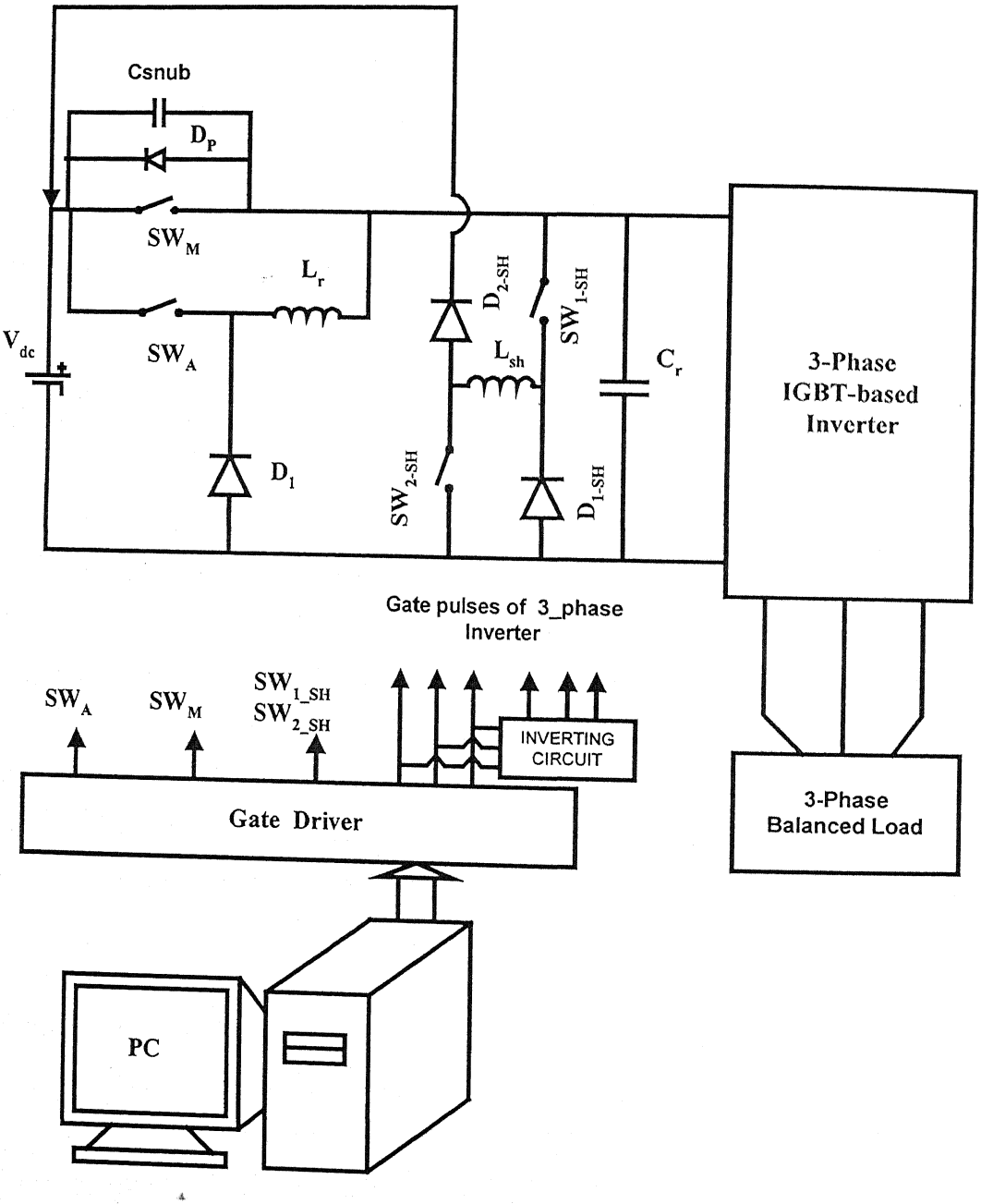


Fig. 4.10. Hardware Implementation

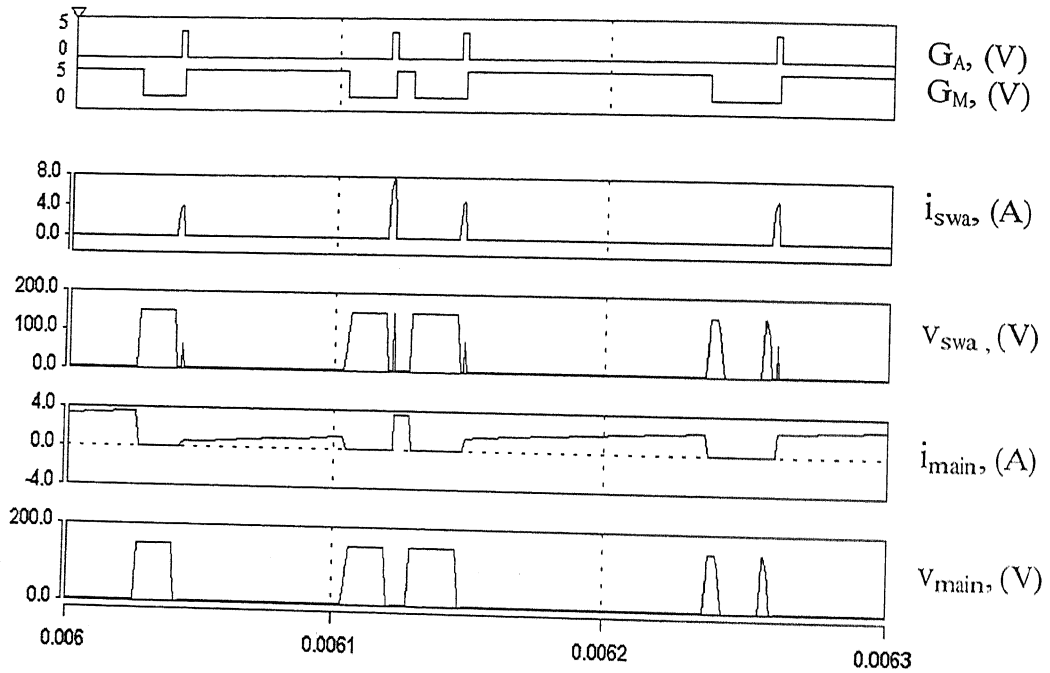
4.7 Simulation Studies

The QRDCL inverter is modeled and simulated by SABER for R-L-load with the following data:

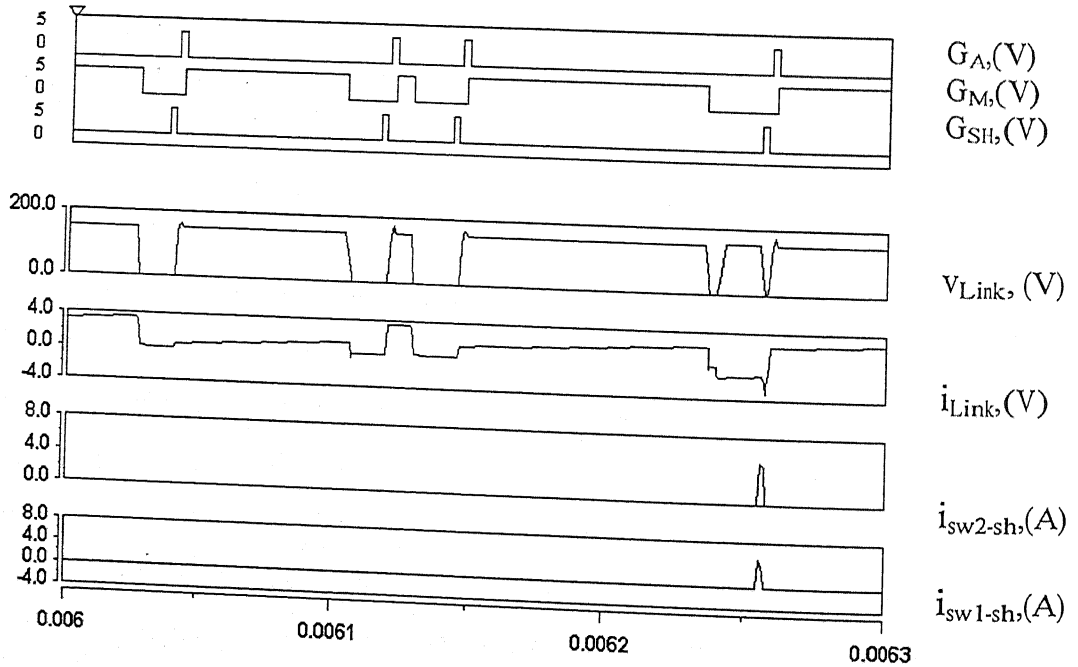
Three-phase balanced load with each phase having $R_d = 10\ \Omega$, $L_d = 6.89$ mH
Output fundamental frequency = 400 Hz
Power factor = 0.5 lagging
Modulation index = 0.7.
Resonant circuit parameters: $L_r = 8\mu H$, $L_{sh} = 6\ \mu H$ and $C_r = 20$ nF.
DC Supply voltage = 150 V.
Switching frequency of the link = 14.38 kHz ($T_s = 69.5\ \mu s$)

A few typical waveforms obtained from simulation are shown in Fig. 4.11. The current and voltage across the auxiliary switch SW_A and the main switch SW_M are shown in Fig. 4.11(a). The main switch is turned on/off under ZVS. The shunt switches are turned on under ZCS and turned off under ZVS. The auxiliary switch turns on under ZCS, but turns off hard. In Fig. 4.11(b), it is observed that the link voltage is clamped to the source voltage at some interval when the gate pulses to the switches SW_A and SW_M are not present. Under this condition the link current is negative as may be seen from the waveform of the link current. It is essential to discharge the resonant capacitor before soft-switching transition is undertaken. This is achieved by closing the shunt switches. After the link voltage drops to zero owing to discharge of resonant capacitor, the turn-on and turn-off of switching devices in the inverter are operated under ZVS. The currents through various components are shown in Fig. 4.11(c-d). Figure 4.11(d) shows input current (i_{Link}) to the inverter and current (i_{Dp}) through the anti-parallel diode D_p when the auxiliary switch SW_A is turned off. The voltage across the switch S_{an} of phase-a of the inverter, and the current flowing through it are shown in Fig. 4.11(e). The gate pulses for the switches in the resonant link within a sector and the corresponding link voltage are shown in Fig. 4.11(f). The three-phase currents flowing from the QRDCL inverter and the line-to-line voltage (V_{ab}) with MSVM are shown in Fig. 4.11(g). It is observed that the three-phase output currents of the

inverter are sinusoidal.

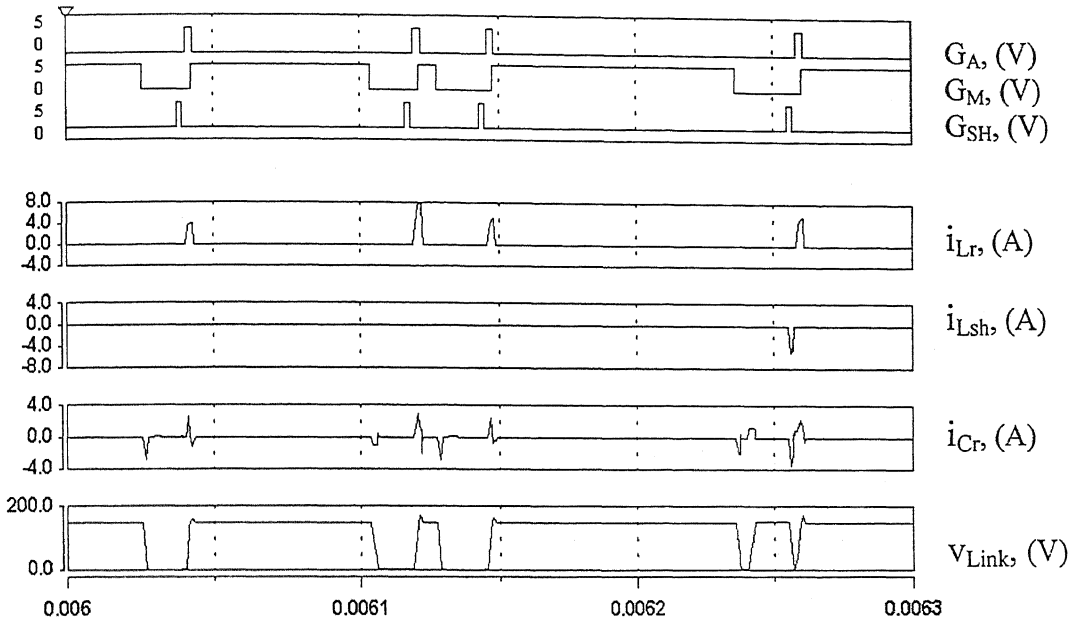


(a)

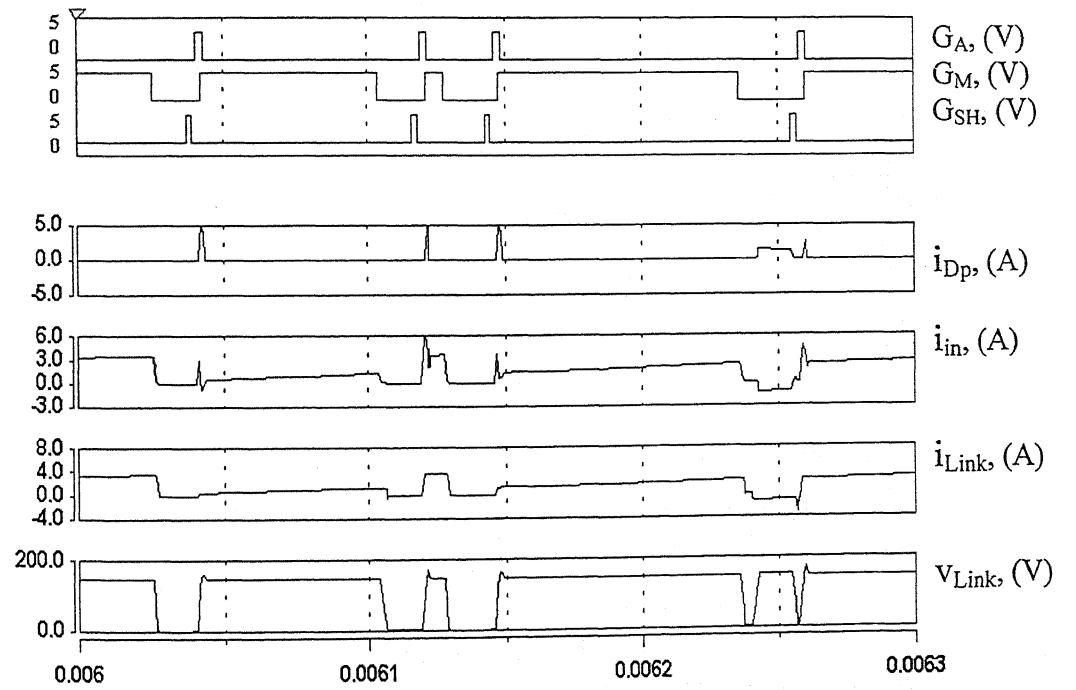


(b)

Fig. 4.11 Contd.



(c)



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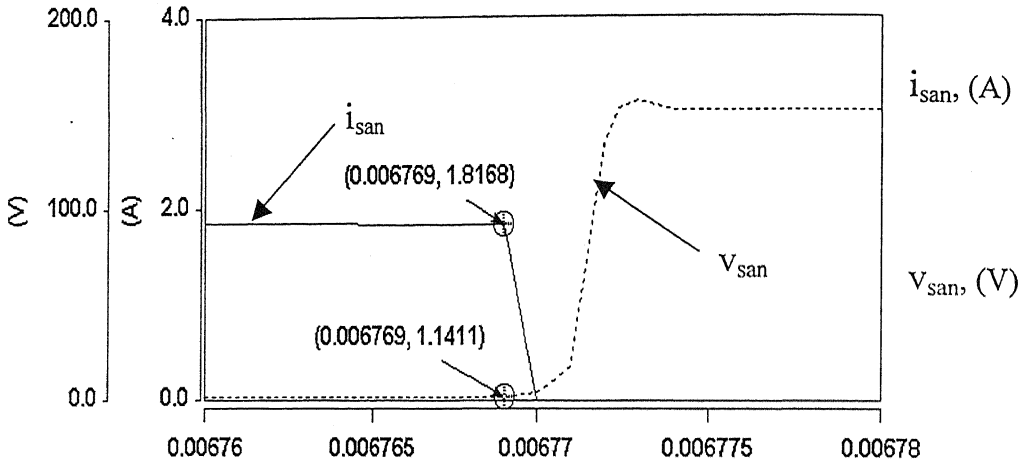
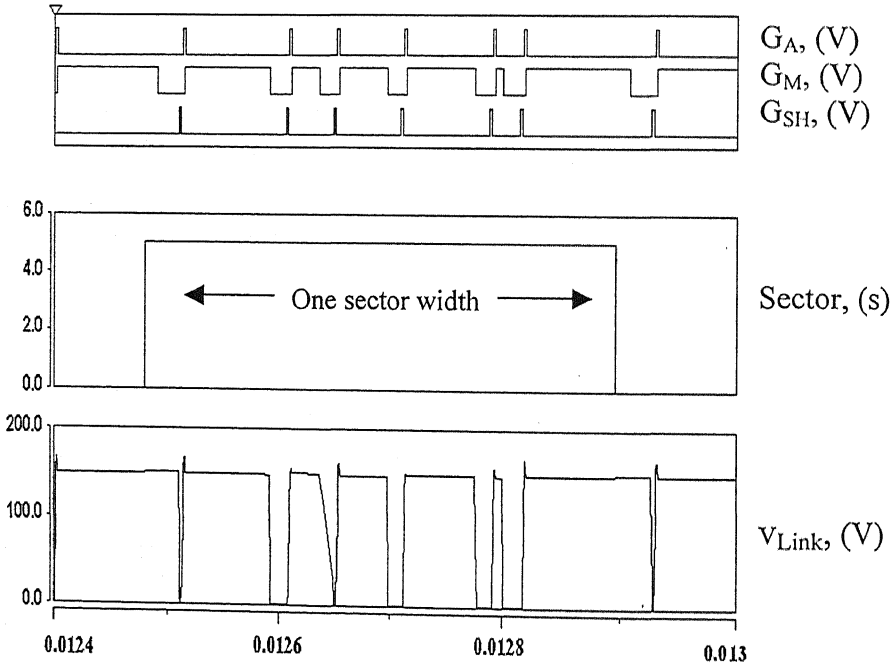
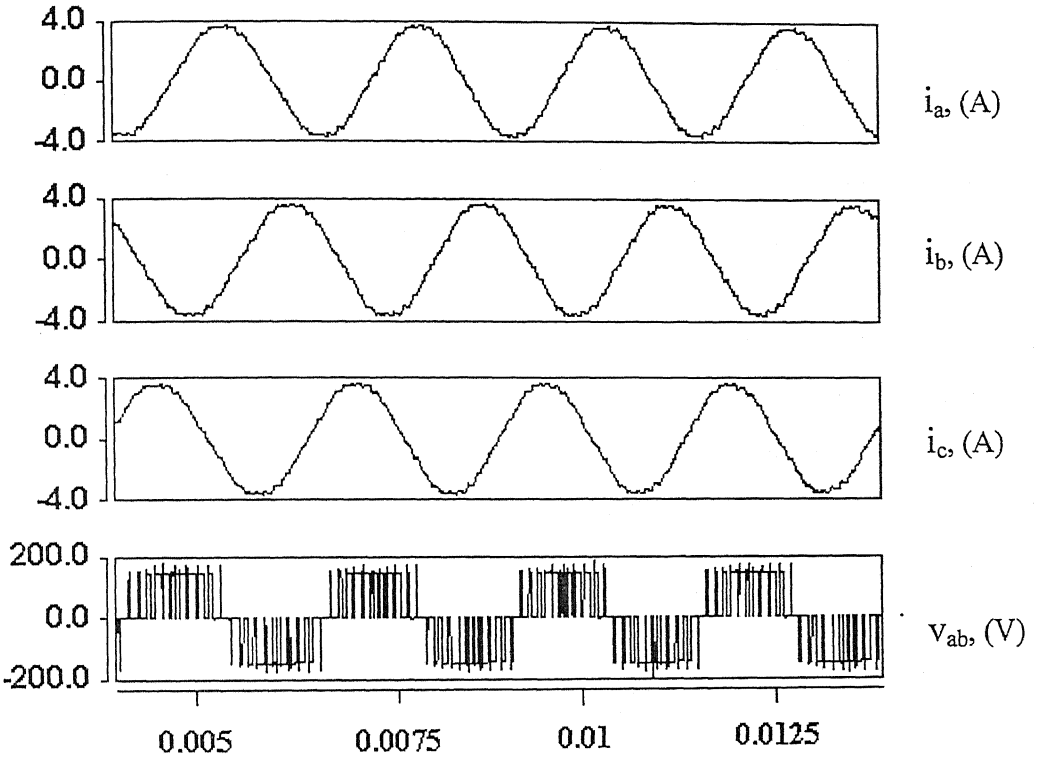


(e)



(f)

Fig. 4.11 Contd



(g)

Fig.4.11: Simulation results at $T_s = 69.5$ μs, (i.e., 14.38 kHz), modulation index = 0.7, fundamental frequency = 400 Hz, static load parameters per phase ($R_d = 10\Omega$, $L_d = 6.89$ mH) and power factor = 0.5

G_A, G_M, G_{SH}: Gate signals of auxiliary switch (SW_A), main switch (SW_M) and pair of shunt switches ($SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$).

(a) Currents and voltage across the auxiliary switch (SW_A) and main switch (SW_M)
((b)-(d)): Various waveforms across different components of quasi-resonant inverter.
(e) Voltage and current of the inverter switch (SW_{an})
(f) Gate pulses in a sector and link voltage.
(g) Three-phase output currents of inverter and line-to-line voltage.

The performance of the quasi-resonant link inverter with MSVM is shown in Tables 4.1- 4.4. Table 4.1 shows efficiency and THD with three values of switching frequency. The efficiency decreases slightly and THD decreases as switching frequency is increased. This shows that losses with increase with an increase in the switching frequency due to increase in the conduction losses. With increasing switching frequency, the output currents have less THD and they tend to be more sinusoidal. Tables 4.2 and 4.3 show the variation of efficiency and THD with increasing values of resonant parameters; Table 4.2 shows for the resonant capacitor while Table 4.3 shows for the resonant inductor with all other parameters held constant as shown in these tables. The efficiency decreases in both cases. The THD also decreases in both cases, but the decrease is not significant. Table 4.4 shows the effect of increasing load power factor on efficiency and THD. The load impedance is made constant with changing power factor angle. The efficiency is almost constant with power factor variation from 0.5 to 0.8. The THD, however, increases significantly with an increase in power factor.

Table 4.1 Percentage of efficiency and THD of QRDCL inverter at various switching frequencies

Performance of resonant link inverter at different switching frequencies with the following fixed parameters and power ***factor of 0.5.*** *(R_L = 10Ω, L_d = 6.89 mH, L_r = 8μH, L_{sh}= 6μH, Cr=20 nF) Fundamental frequency = 400 Hz*		
Switching frequency (kHz)	Efficiency (%)	THD %
9.615	94.1	7.3
14.38	93.38	5.2
19.23	92.01	4.4

Table 4.2 Percentage of efficiency and THD of QRDCL inverter at various values of resonant capacitors

Performance of resonant link inverter at various values of ***resonant capacitors*** *with the following fixed parameters and* ***power factor of 0.5.*** *(R_L = 10Ω, L_d = 6.89 mH, L_r = 8μH, L_{sh}= 6μH) Fundamental frequency = 400 Hz Switching frequency = 9.615 kHz*		
Resonant capacitor Cr (nF)	Efficiency (%)	THD %
20	94.1	7.3
40	92.04	7.01
60	90.43	6.89

Table 4.3. Percentage of efficiency and THD of QRDCL inverter at various values of resonant inductors

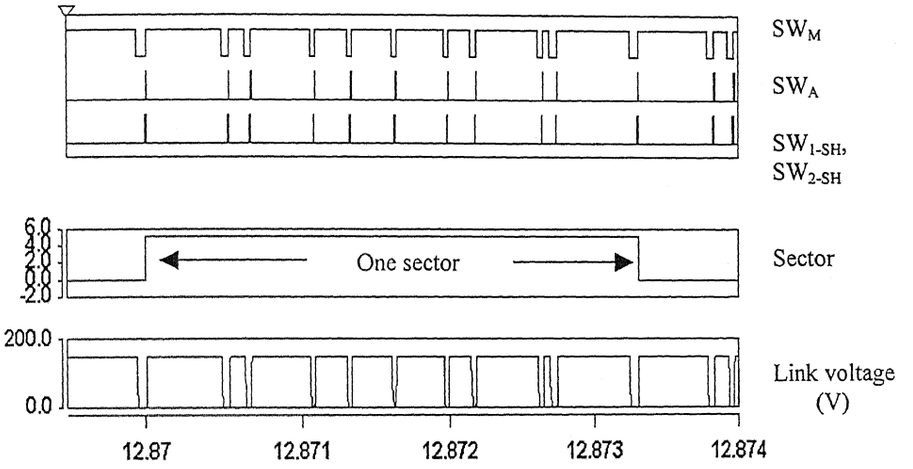
Performance of resonant link inverter at various values of ***resonant inductors*** *with following fixed parameters and* ***power factor of 0.5.*** *(R_L = 10Ω, L_d = 6.89 mH, L_{sh}= 6μH, C_r = 20 nF) Fundamental frequency = 400 Hz Switching frequency = 9.615 kHz*		
Resonant Inductors Lr (μF)	Efficiency (%)	THD %
8	94.1	7.3
12	93.37	7.03
16	93.0	6.98

Table 4.4. Percentage of efficiency and THD of QRDCL inverter at various values of load power factor

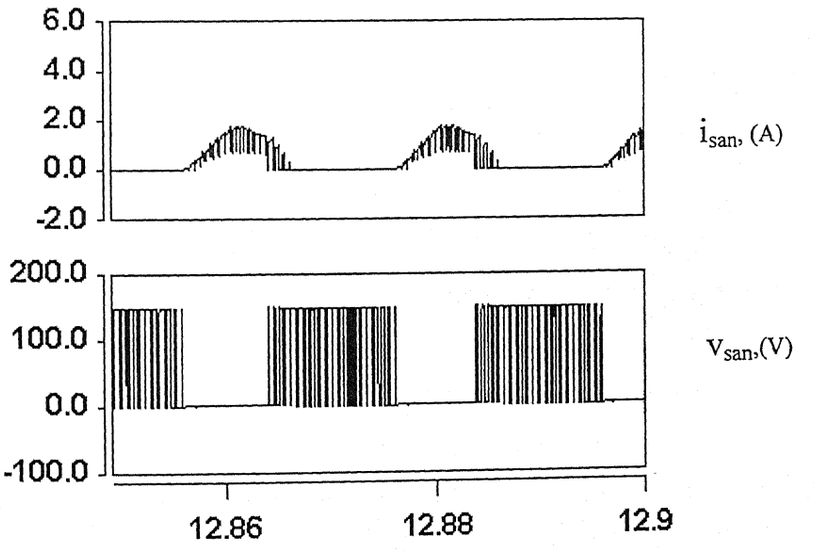
Performance of resonant link inverter at various values of ***power factor*** *with fixed load impendence and the following fixed parameters. (L_r = 8μH, L_{sh}= 6μH, C_r = 20 nF) Load impedance = 20 Ω, Fundamental frequency = 400 Hz Switching frequency = 9.615 kHz (T_s = 104 μs)*		
Power factor	Efficiency (%)	THD %
0.5	94.1	7.3
0.7	93.7	8.6
0.8	94.38	9.8

The simulation is extended an induction motor load. In this case, the switching frequency of 3.03 kHz (T_s = 330 μs), fundamental frequency of 50 Hz and modulation index of 0.8 are chosen. Figure 4.12 shows some typical simulation results. The gate pulses for the link switches in a sector and the corresponding link voltage are shown in Fig. 4.12(a). The current in the switch S_{an} of the inverter (a-phase) and the voltage across it are shown in Fig 4.12(b). The enlarged figure of Fig. 4.12(b) is shown in Figs. 4.12(c) to demonstrate soft-switching of devices in the inverter. The simulated phase current and line-to-line voltage using MSVM are shown in

Fig. 4.12(d). It is observed that the phase current of the induction motor is close to sinusoidal at low switching frequency.



(a)



(b)

Fig. 4.12 Contd.

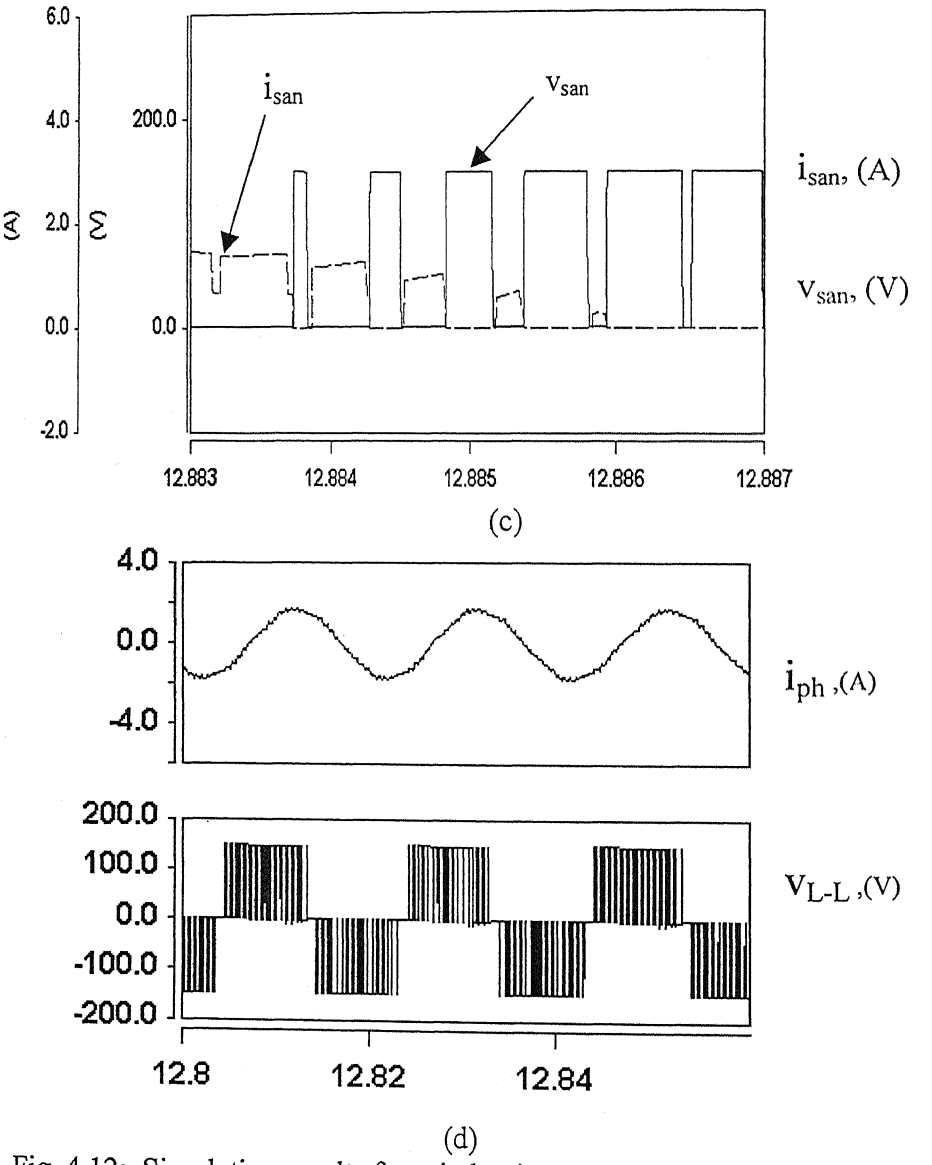


Fig. 4.12: Simulation results from induction motor as load
(Switching frequency= 3.03 kHz, fundamental frequency= 50 Hz, Modulation Index = 0.8)

(a) Gate pulses and Link voltage in a sector

(b) Current and voltage across S_{an} (switch in a-phase of an inverter).

(c) Expanded wavefom of (b). (d) Phase current and line-to-line voltage

4.8 Experimental Results

A laboratory-sized model is fabricated and experimentally tested to compare the simulation under identical operating condition for both static and active load (induction motor load). The following data are considered for static R-L-load during both simulation and experimental setup.

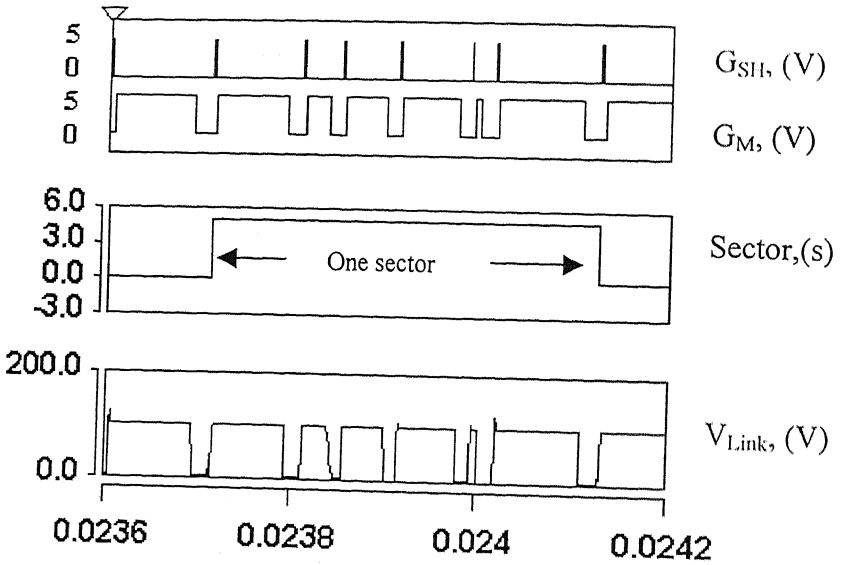
Three-phase balanced load, each phase having $R_d = 8\ \Omega$, $L_d = 4.2$ mH

Switching frequency = 14.38 kHz, Modulation index = 0.7

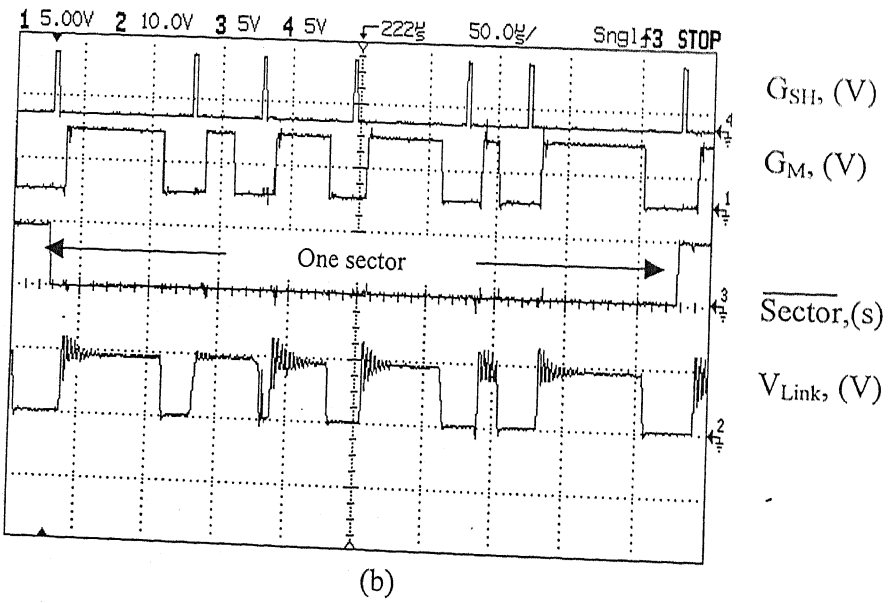
Fundamental frequency = 400 Hz, Load power factor = 0.6

Input dc voltage = 100 V

The experimental results along with corresponding results from simulation are presented in Figs. 4.13-4.17. The gate signals G_{SH} for shunt switches ($SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$), G_M for main switch SW_M and the corresponding dc link voltage obtained from simulation and experiment in one sector are presented in Fig. 4.13. Figures 4.14 - 4.16 show the current and voltage waveforms across the switches SW_A, SW_M, and $SW_{2\text{-}SH}$ respectively. In Fig. 4.14, it is observed that the auxiliary switch SW_A is turned on under ZCS and turned off under hard-switching. Figure 4.15 shows the current and voltage across the main switch SW_M. However, the experimental results show ringing oscillations during turn-on of the main switch SW_M. The results obtained from simulation and experiment agree with each other. It is also seen that the switch SW_M is turned on/off under ZVS. The shunt-switch $SW_{2\text{-}SH}$ is turned on under ZCS and turned off under ZVS as shown in Fig. 4.16. Further, it is noticed that the voltage stress across this switch is reduced to half of the source voltage when the device is not conducting. The current and voltage across the switch $SW_{1\text{-}SH}$ is similar to that of switch $SW_{2\text{-}SH}$. This is, however, not shown here. The input current to the quasi-resonant link inverter and the line-to-line output voltage of the inverter are shown in Fig. 4.17. It may be seen that the dc link current becomes negative for a short interval. Figure 4.18 shows the phase current and line-to-line voltage. The phase current obtained from both simulation and experiment are found to be close to sinusoidal. The theoretical and experimental values of efficiency are 93% and 91% respectively, whereas the theoretical and experimental values of THD for the output current are 4% and 5.5% respectively for the static R-L-load.



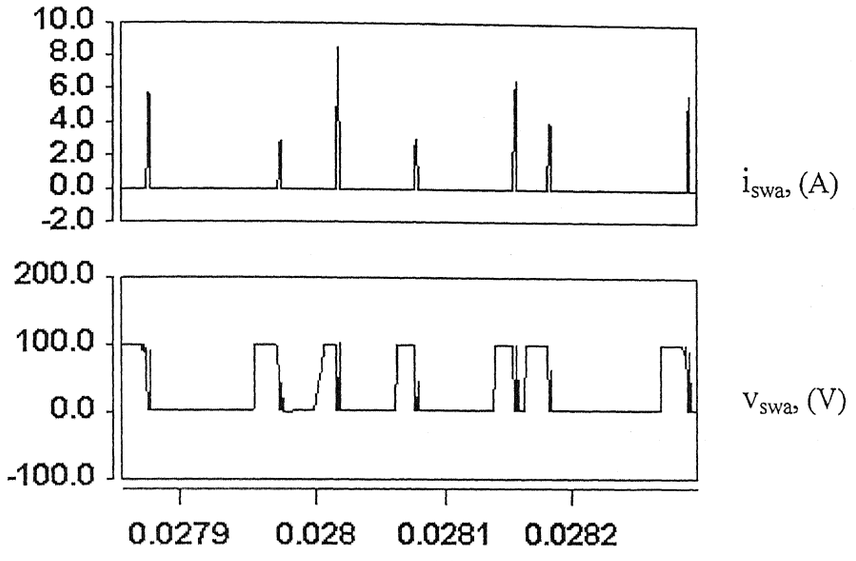
(a)



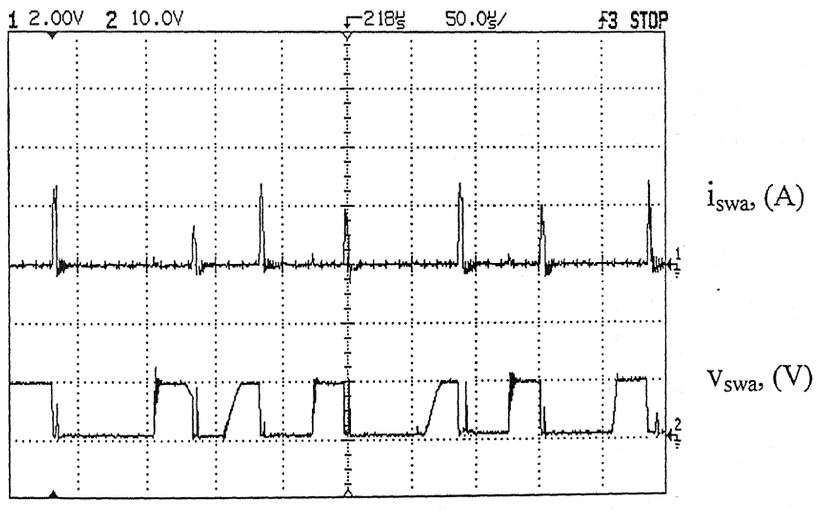
(b)

Fig. 4.13: Gate pulse G_M for switch SW_M, and G_{SH} for shunt switch ($SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$) and dc link voltage in a sector for RL-Load at $T_s = 69.5$ µs, modulation index = 0.7, fundamental frequency = 400 Hz, power factor = 0.6, per-phase load parameters: $R_d = 8\Omega$, $L_d = 4.2$mH.

(a)Simulation result (b) Experimental result (V_{Link} = 1:10)

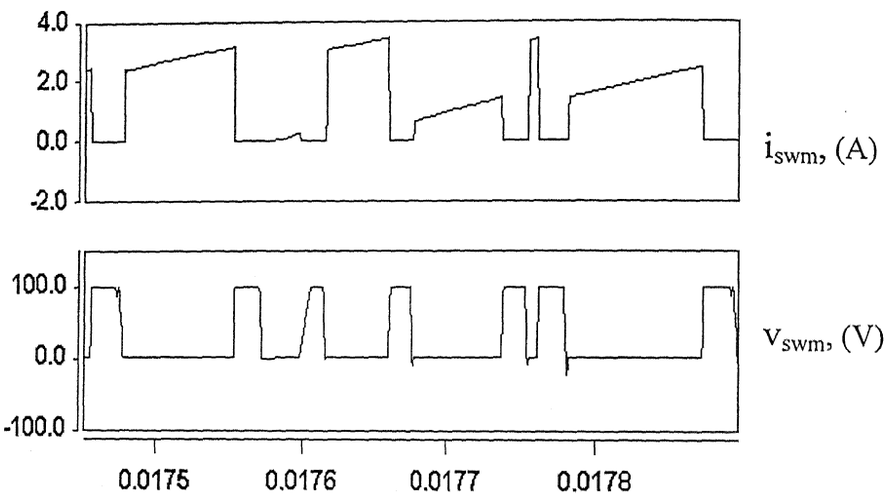


(a)

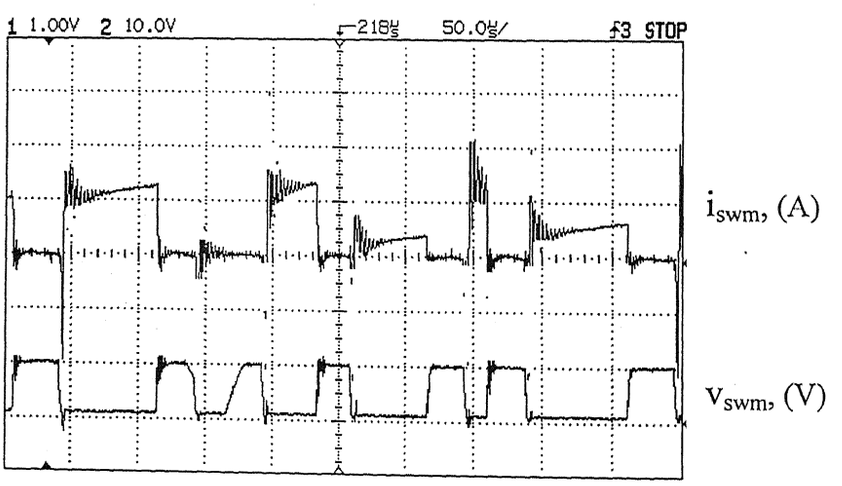


(b)

Fig. 4.14: Current (i_{swa}) through and voltage (v_{swa}) across the auxiliary switch SW_A. (T_s = 69.5 µs, modulation index = 0.7, fundamental frequency = 400 Hz, power factor = 0.6)
(a)Simulation result (b) Experimental result (Scale:i_{swa}:- 2A/V, v_{swa}: 1:10)



(a)

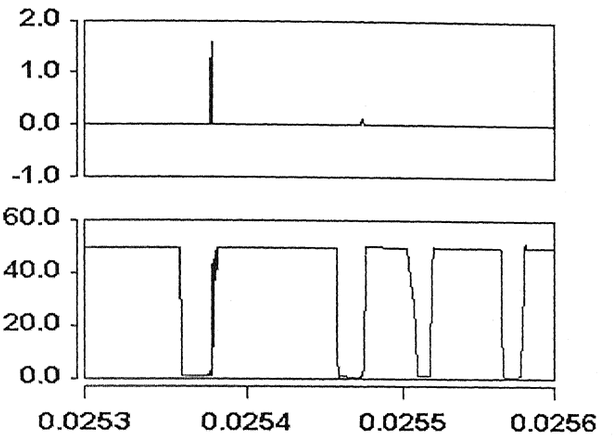


(b)

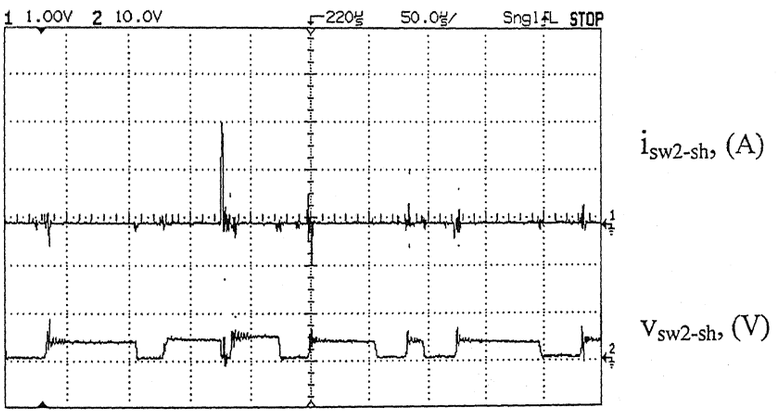
Fig. 4.15: Current (i_{swm}) through and voltage (v_{swm}) across the main switch (SW_M). (T_s = 69.5 µs, modulation Index = 0.7, fundamental frequency= 400 Hz, Power factor = 0.6) for static R-L-load

(a) Simulation Result

(b) Experimental Result (scale: i_{swm} -2A/V, v_{swm} - 1:10)



(a)

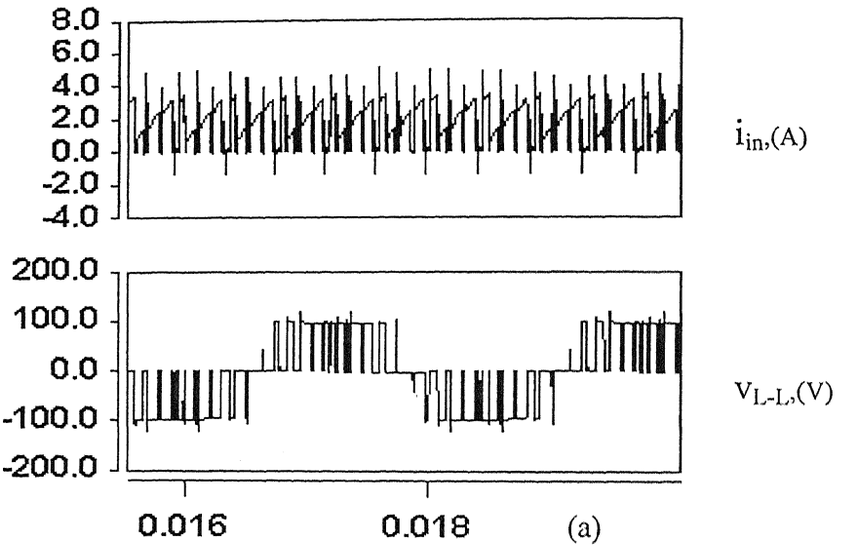


(b)

Fig. 4.16: Current ($i_{sw2\text{-}sh}$) and voltage ($v_{sw2\text{-}sh}$) across the shunt switch $SW_{2\text{-}SH}$. (T_s = 69.5 µs, modulation Index = 0.7, Fundamental frequency= 400 Hz, Power factor = 0.6)

(a) Simulation result

(b) Experimental result, (scale: $i_{sw2\text{-}sh}$: 2A/V, $v_{sw2\text{-}sh}$ 1:10)



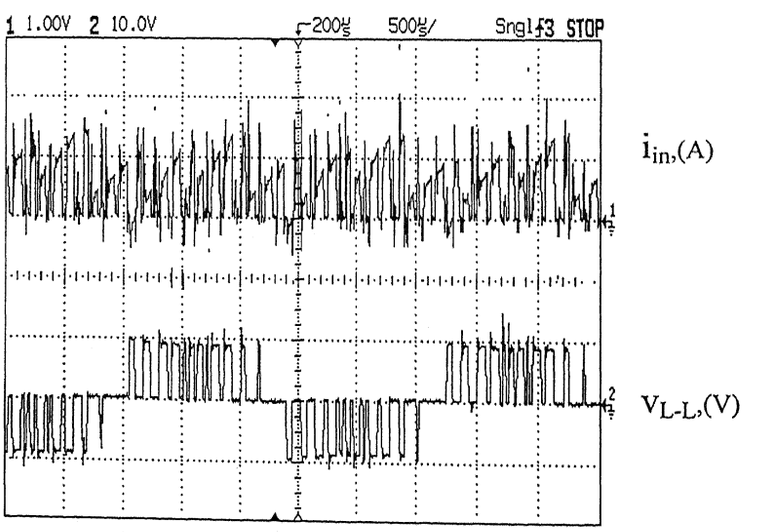


Fig.4.17: Input current (i_{in}) to quasi-resonant link topology and line-to-line voltage (V_{L-L}) across the output of inverter.(T_s = 69.5 μs, modulat -ion Index = 0.7, Fundamental frequency= 400 Hz, Power factor = 0.6)

(a) Simulation result

(b) Experimental result (scale: i_{in} - 2A/V, V_{L-L}-1:10)

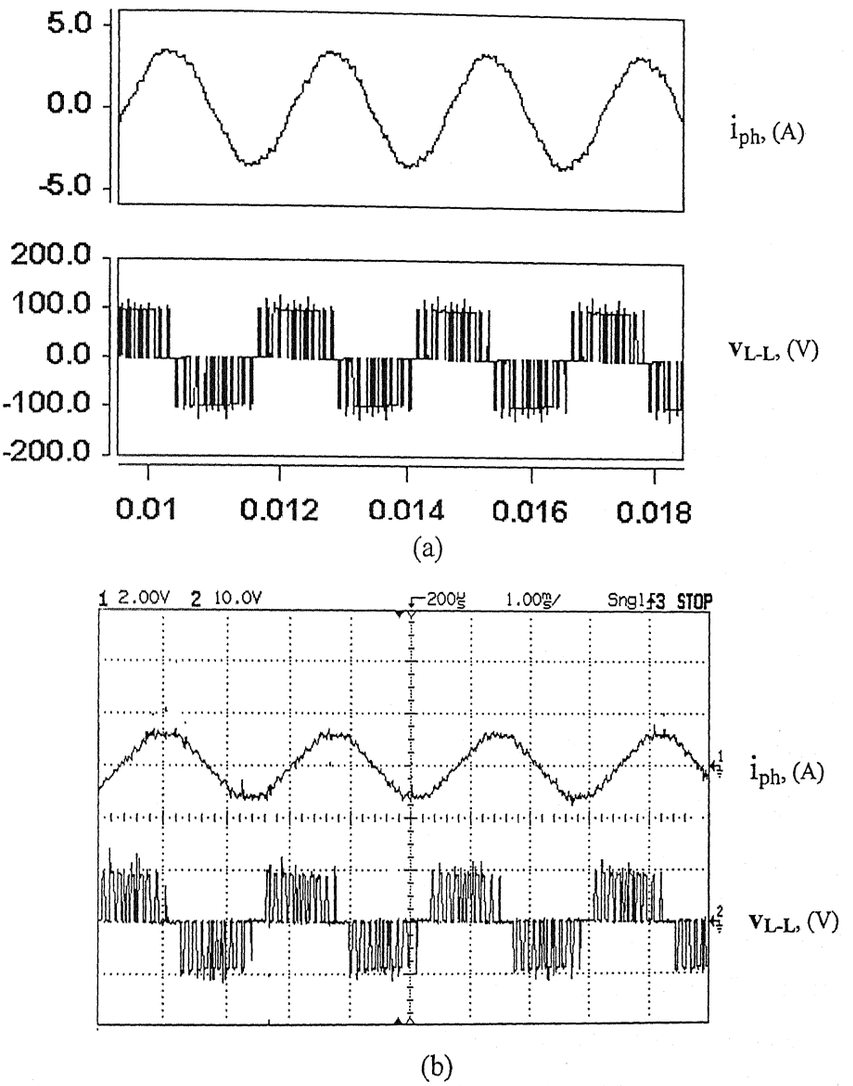


Fig. 4.18: Phase current (i_{ph}) and line-to-line voltage(v_{L-L}) for static RL-Load at T_s = 69.5 μs, Modulation Index = 0.7, Fundamental frequency =400 Hz, Power factor = 0.6
Per-phase load parameters (R_d = 8Ω, L_d= 4.2mH)

(a) Simulation result

(b) Experimental result (Scale: i_{ph}- 2A/V, v_{L-L} -1:10)

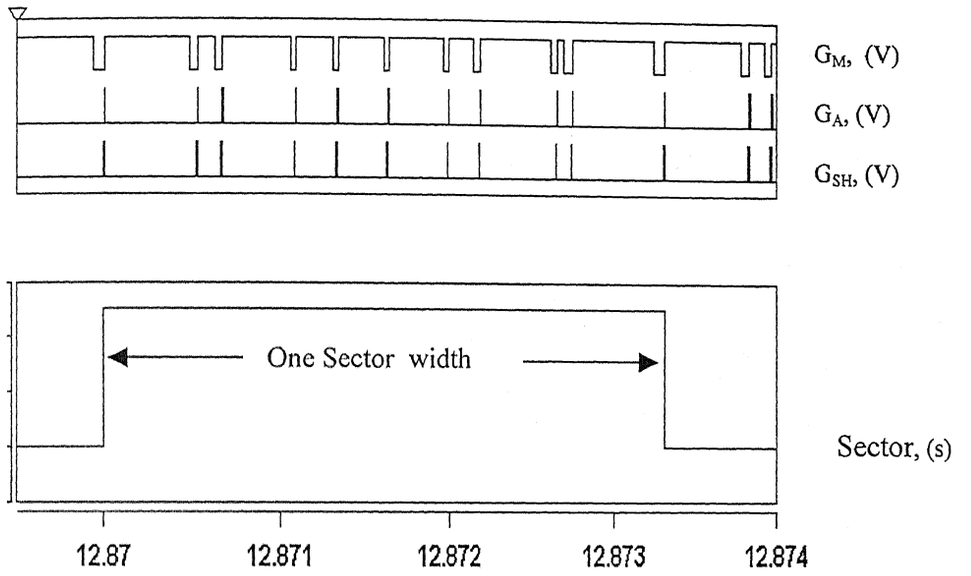
The experiment is extended to induction motor load. The induction motor used in this experiment is of smaller VA rating. The parameters of the induction motor are given in Appendix-C. The other parameters in the experiment are the same as those assumed in simulation and mentioned in the following:

Switching frequency = 3.3 kHz
Modulation index = 0.8
Input dc voltage = 150 V
Fundamental frequency = 50 Hz.

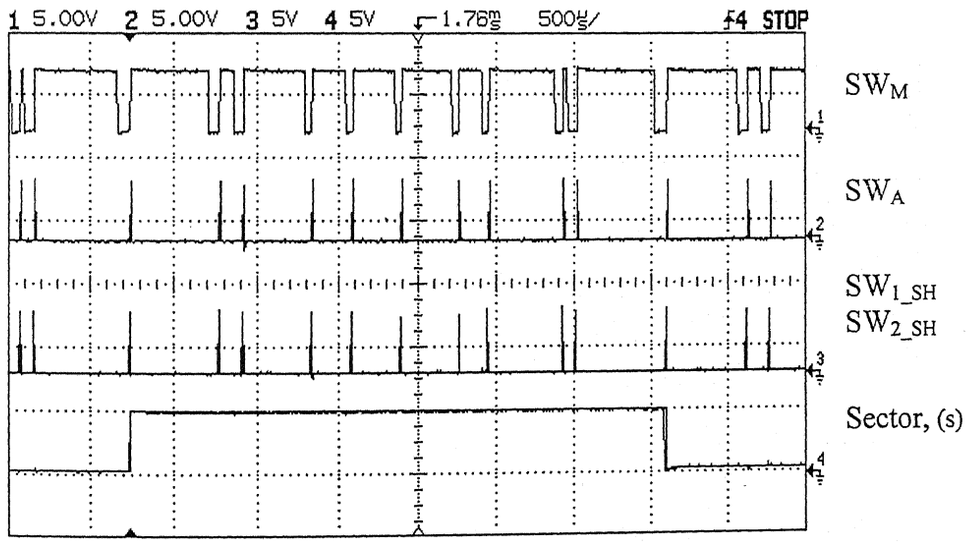
The experimental results along with the simulation results are presented in Figs. 4.19-4.22. The gate signals for the switching devices of the resonant dc link SW_M, SW_A, $SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$ obtained from simulation and experiment for one sector are shown in Fig.4.19 (a) and Fig. 4.19(b) respectively.

Figure 4.20 shows both simulation and experimental results of the link voltage with respect to gate signals of switching devices in the dc link with the exception of gating pulse for the auxiliary switch.

It may be seen that the waveform of the dc link voltage matches with turn-on and turn-off pulses of the main switch. Soft-transition of switching devices in the inverter is achieved during the interval when the dc link voltage is zero. The steady state waveforms of the phase current i_a and the line-to-line voltage v_{ab} by simulation and experiment are shown in Fig. 4.21(a) and Fig. 4.21(b) respectively. There is a good match between simulation and experimental results. Even at low switching frequency of 3.03 kHz, the MSVM technique produces balanced three-phase current which are close to sinusoidal. This can be seen from the waveforms of the current in phase-a (Fig. 4.21). The harmonic analysis of the phase 'a' current is carried out both for simulation and experiment. The amplitudes of harmonics up to 9^{th} obtained by both simulation and experiment are shown in Fig. 4.22. It is observed that there is a slight discrepancy in the amplitude of fundamental and other harmonics. The discrepancy in amplitudes of the fundamental component (Fig. 4.22) may be due to the differences between the measured parameters and physical parameters of the induction machine.

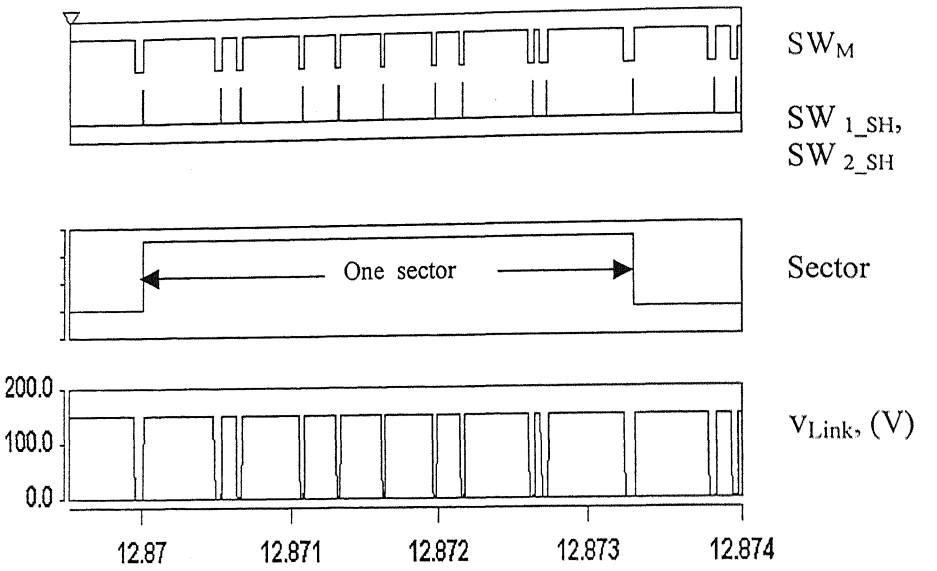


(a)

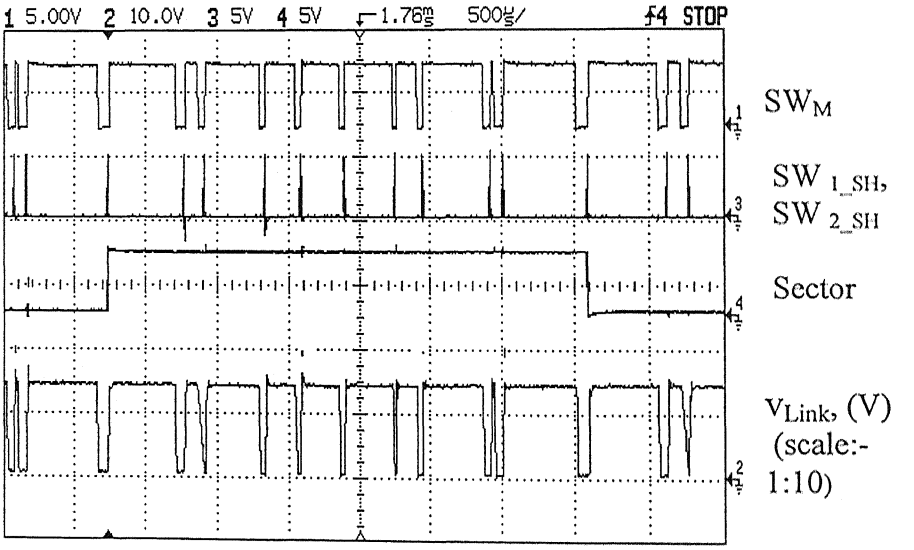


(b)

Fig. 4.19 Simulated and experimental results for induction motor load
(i.e., Gate pulses of link switches in a sector)
(a) Simulated results (b) Experimental results

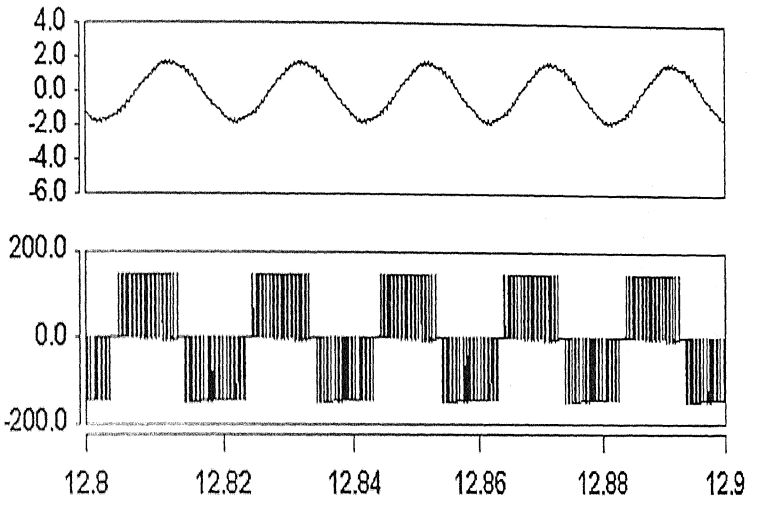


(a)

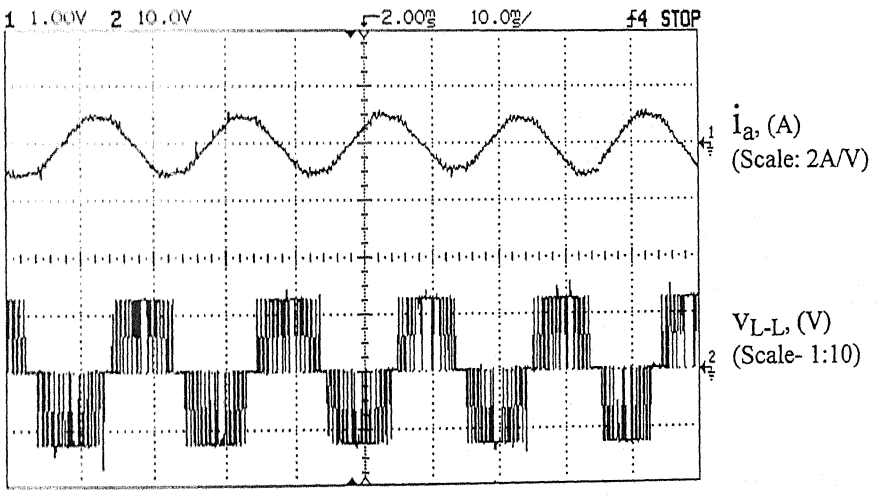


(b)

Fig.4.20: Simulated and Experimental results from induction motor load.
(Gate signals and link voltage in a sector)
(a) Simulated results (b) Experimental Results



(a)



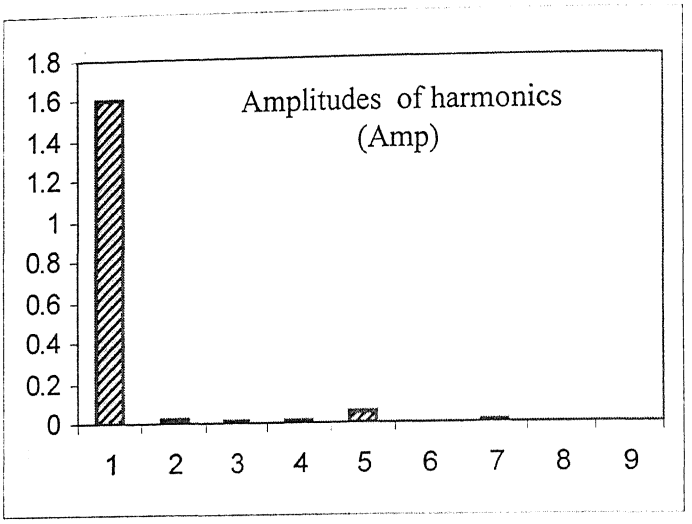
(b)

Fig. 4.21: Simulated and experimental results from induction motor load.

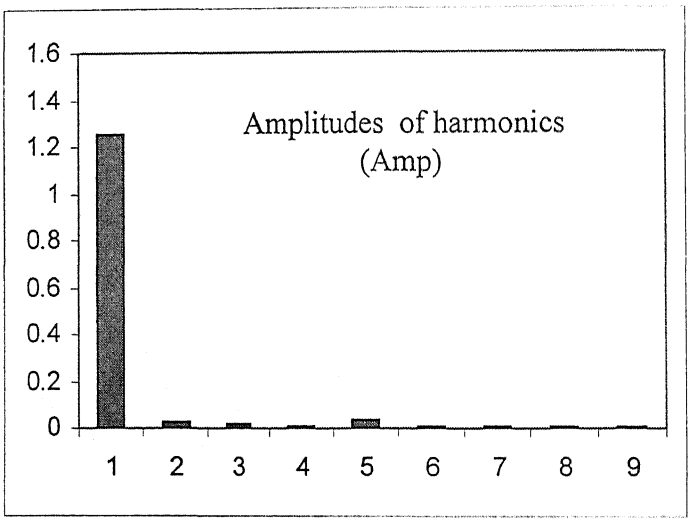
(i.e., phase current (i_a) and line-to-line voltage (V_{L-L}))

(a) Simulated results

(b) Experimental results



(a)



(b)

Fig. 4.22. Harmonic analysis of a-phase current from induction motor load.
(a) Simulation
(b) Experimental setup

The THD and efficiency obtained by simulation and experiment for induction motor load as shown in Table 4.5.

Table 4.5

	Simulation	Experiment
THD	6%	8%
Efficiency	96%	91%

The waveforms of output phase currents have further improved when the switching frequency is doubled from 3.03 kHz to 6.06 kHz while keeping other parameters constant. This is demonstrated by the experimental results for the phase current (i_a) and line-to-line voltage (v_{ab}) as shown in Fig. 4.23.

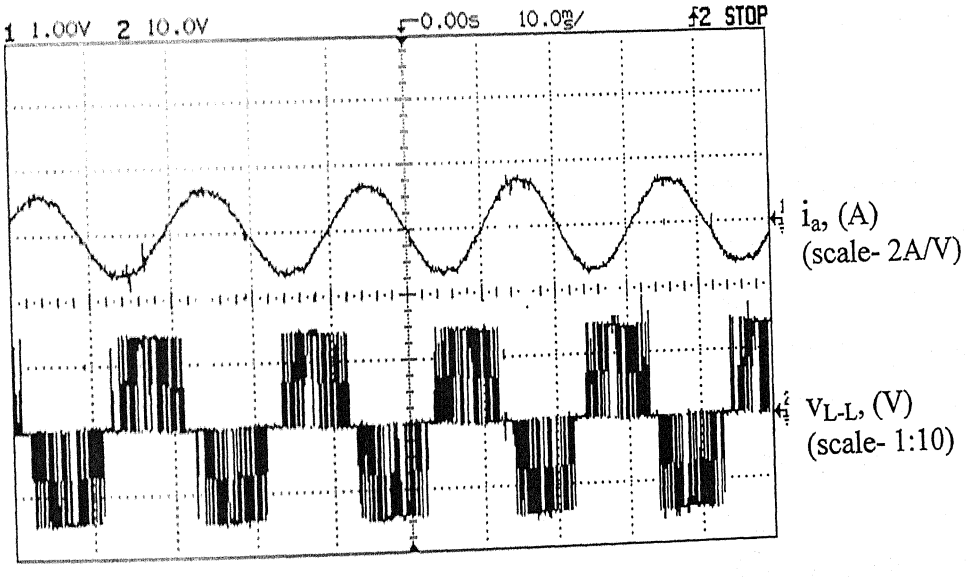


Fig. 4.23: Experimental results of phase current (i_a) and line-to-line voltage (v_{ab})) from induction motor load at T_s = 165μs,(f_s = 6.06 kHz), modulation index = 0.7.

4.9 Conclusion

The new quasi-resonant inverter topology proposed in this chapter is simulated and experimentally verified. The switching sequence of various switches in the resonant link is formulated to permit soft-switching of switches in the inverter. Several modes of operation have been identified for soft-switching transition of devices in the same leg of the inverter when the dc link current is positive. The number of modes has increased further when the link current is negative. Soft-switching of inverter devices is ensured independent of the direction of current in the dc resonant link by the resonant link topology and its control strategy. The quasi-resonant link inverter presented in this chapter is quite adaptable for both low and high power factor loads. The detailed simulation of quasi-resonant inverter topology along with MSVM technique using SABER simulator and subsequent experimental verification with both R-L and induction motor load show good agreement.

CHAPTER 5

A Quasi-Resonant Inverter-fed High Performance Induction Motor Drive System

5.1 Introduction

Induction motors are widely used in industries because of their simplicity, ruggedness and robustness. Variable voltage and variable frequency (VVVF) operation is generally used for speed and torque control of induction motor drives. The literature related to ac drives covering scalar control, field-oriented control, and direct-torque control (DTC) has been well documented [46]. Compared to scalar control and vector/field-oriented control, the direct torque control scheme is known for its fast transient response and simplicity of implementation owing to absence of current control, traditional PWM algorithm and vector transformation. High performance induction motor drives employing DTC strategies have been reported in the literature [47-52]. Nash [47] reported that direct torque control combines the benefits of direct flux and direct torque control into a sensorless variable-frequency drive that does not require a PWM modulator. A new quick response and high-efficiency control of an induction motor, which is quite similar to direct torque control, was initially proposed in [48]. Depenbrock [49] proposed the idea of direct self-control (DSC) and defined that DSC is a simple method of signal processing which gives converter-fed three-phase machines an excellent dynamic performance. The torque ripple reduction technique of DTC for high power induction motors driven by three-level inverters has been reported in [50] where the inverter switching frequency has been limited to around 0.5-1 kHz. A direct flux and torque control scheme for industrial application has been analyzed in [51] emphasizing the drive performance at standstill and in low speed range. A new speed-sensorless DTC of induction motor drive is presented in [52]. In all these schemes, a better torque profile and current response have been focused.

The flux observer of induction motor drive is very important as far as the dynamic performance of the drive is concerned. The flux observer should give a correct flux estimate with

varying operating conditions. The different techniques of flux observer have been put forth in the literature [52-54]. The drive in [52] uses an adaptive flux observer for speed estimation, and a discrete-time direct torque control technique for torque and stator flux control. In [53,54], the authors have reported a reduced order stator flux observer for a cycloconverter-fed vector controlled synchronous motor drive. The observer designed has been found to be robust against speed variation.

The improved performance at various levels of ac drives as mentioned above is obtained at the cost of high switching losses because of hard-switchings in conventional PWM inverter. Additionally, the windings of induction motor are subjected to high switching stresses. Consequently, insulation between the inter-turn layers of the windings of induction motor get weakened and this reduces the durability of the machine. Above all, it is to be noted that the hard-switchings in PWM inverter not only result in the limitations of the inverter (i.e., EMI, increase in losses, weight and volume of inverter), but also do harm to the induction motor. To overcome these problems, soft-switching strategies [16] have been actively considered in recent times for the inverter-fed induction motor drives. As a result, the switching losses are reduced, thereby increasing the overall efficiency in addition to improved drive performance.

In the area of soft-switching inverter-fed induction motor drives, only a few papers [28, 32, and 45] have appeared recently in the literature. The authors in [28] have reported a three-phase soft-transition inverter-fed induction motor drive operating in a closed-loop speed/torque control. This inverter requires additional inverter and LC components in each phase for implementation of soft-switching. A novel technique using the resonant snubber-based principle has been proposed in [32] for propulsion drives. The control technique in this case is standard sinusoidal PWM method, which requires a reference sinusoidal wave to be compared with a triangular carrier wave so as to generate the desired signals for switching devices. The circuit uses one resonant switch, one diode, and one resonant inductor in each phase of the three-phase load in addition to the three-phase inverter. These additional components are connected in star/delta arrangement across the three-phase load circuit to realize soft switching of inverter devices. A soft-switched inverter with fixed frequency bang-bang current control technique has been implemented to sinusoidally shape the phase currents of the induction motor [45]. One of the

switches in the resonant link and all switches in the inverter suffer from turn on stresses. Hence, the scheme is under partial soft-switching. Thus, a soft-switching inverter-fed three-phase high performance induction motor drive is lacking in the literature. Therefore, a novel soft-switched quasi-resonant inverter-fed three-phase induction motor under DTC is considered here for detailed investigation. The scheme is further extended to include a robust, reduced order stator flux observer. The d-q model of the complete scheme is formulated and its performance is analyzed by SABER simulator. A laboratory-sized model is fabricated and experimentally tested to validate the simulation results under identical operating conditions.

The basic concepts of conventional DTC scheme are reviewed briefly in the next section before discussing the DTC scheme employing quasi-resonant inverter.

5.2 Direct Torque Control (DTC) Scheme

The conventional DTC scheme for an induction motor is shown in Fig. 5.1 where the major part of the control scheme is implemented by software control except some hardware comprising of sensors and device drivers. The dotted portion marked in Fig. 5.1 shows the operation under software control by a PC. The developed torque of the machine (T_e) is proportional to the product of synchronously rotating stator flux Ψ_s, rotor flux Ψ_r, and sine of the angle (δ) between them. In a PWM inverter-fed machine, the vector Ψ_r is filtered more than Ψ_s and therefore, Ψ_r vector rotates more smoothly. The motion of Ψ_s, dictated by the impressed voltage vector is discontinuous, but its average velocity is the same as that of Ψ_r in the steady state. In the DTC scheme, the magnitude of Ψ_s is controlled within a hysteresis band by the voltage vector so as to obtain a flux of continuous and constant magnitude. The voltage vectors are similar to the vectors discussed in section 3.4. There are six active non-zero vectors and two zero vectors.

The generalized stator voltage vector (V_s) can be expressed in terms of switching functions S_a, S_b, and S_c. S_a, S_b, and S_c are the status of the switching devices in phases (a, b, and c) of inverter respectively. Their values are either '1' or '0'. Thus, the generalized stator voltage vector is

$$\mathbf{V_s}(S_a, S_b, S_c) = \sqrt{(2/3)}\, V_m \left[S_a + S_b \exp(j2\pi/3) + S_c \exp(j4\pi/3)\right] \quad (5.1)$$

where V_m is the dc link voltage of the inverter.

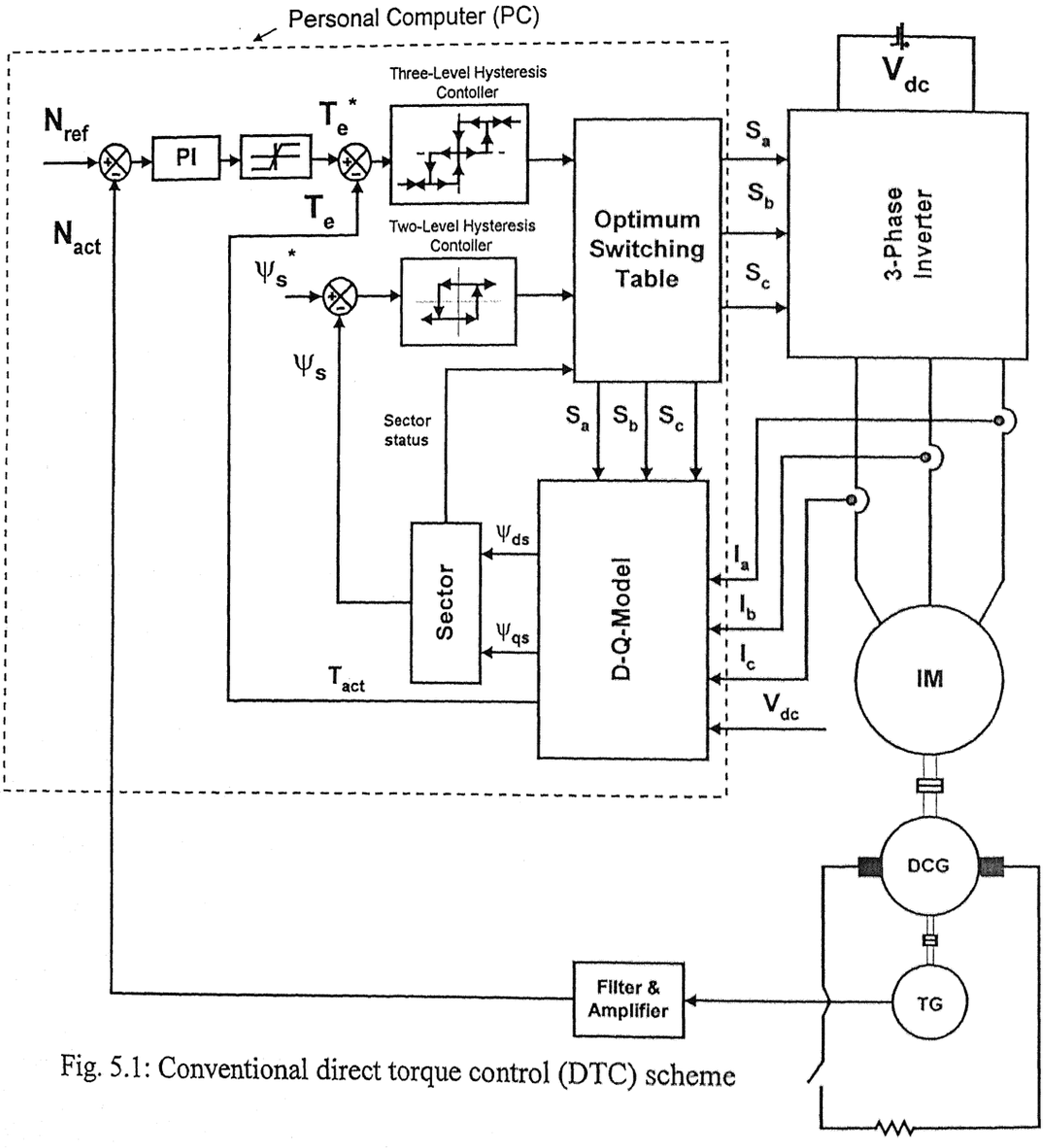


Fig. 5.1: Conventional direct torque control (DTC) scheme

Considering this generalized equation, the six non-zero vectors are $\mathbf{V_s}(1,0,0)$, $\mathbf{V_s}(1,1,0)$, $\mathbf{V_s}(0,1,0)$, $\mathbf{V_s}(0,1,1)$, $\mathbf{V_s}(0,0,1)$, $\mathbf{V_s}(1,0,1)$ and the two zero vectors are $\mathbf{V_s}(0,0,0)$, $\mathbf{V_s}(1,1,1)$. These are similar to voltage space vectors $\mathbf{V_1}$ to $\mathbf{V_6}$ and zero vectors $\mathbf{V_0}$ and $\mathbf{V_7}$ as discussed in section 3.4.

The stator flux linkage Ψ_s is given by the integral of the induced voltage vector behind the stator resistance.

$$\Psi_s = \int (\mathbf{V_s} - \mathbf{i_s}\, r_s)\, dt \tag{5.2}$$

If the voltage drop due to stator resistance $i_s\, r_s$ is neglected, then the trajectory of stator flux is found to move in the direction of the applied stator voltage vector [48]. When the output is one of the active or non-zero voltage vectors, Ψ_s moves at a constant velocity which is proportional to the magnitude of the stator voltage. On the other hand, when a zero voltage vector is selected, the velocity is nearly zero, as the drop in the stator resistance is negligible. Thus, the trajectory of Ψ_s can be made to follow a specified path by a proper choice of stator voltage vectors. The magnitude of Ψ_s is kept constant within a hysteresis band and the rotating velocity is regulated by changing the output voltage vector ratio between zero vectors and active vectors. Thus, a judicious selection of active and zero voltage vectors forms the key to DTC control. Accordingly, the direction of rotation can also be changed. The magnitude of flux is maintained at a constant through a two-level hysteresis controller. The control of flux by the two-level hysteresis controller is based on the following inequality.

$$(\Psi_s^* - \Delta\Psi_s) < \Psi_s \leq (\Psi_s^* + \Delta\Psi_s) \tag{5.3}$$

where Ψ_s^* is the magnitude of the reference stator flux, Ψ_s is the magnitude of the actual flux, and $\Delta\Psi_s$ is the flux band.

Eq. (5.3) is interpreted through software control as follows:

If $\Psi_s \geq (\Psi_s^* + \Delta\Psi_s)$, then $\Psi_{st} = 0$

If $\Psi_s < (\Psi_s^* - \Delta\Psi_s)$, then $\Psi_{st} = 1$

where Ψ_{st} is the status of flux having the value '0' or '1'.

The flux status $\Psi_{st} = 1$ indicates that the actual flux is below the lower limit of hysteresis and the voltage vectors are selected in such a way that the flux level is increased. Similarly, the flux status $\Psi_{st} = 0$ indicates that the actual flux level is beyond the upper limit of hysteresis band and

accordingly the voltage vectors are selected to reduce the flux.

The error between the reference and actual torque is passed through a three-level hysteresis controller to realize torque control in both clockwise and anti-clockwise directions. This is implemented by the following inequalities:

For clockwise rotation: $(T_e^* - \Delta T) \leq T_e \leq T_e^*$ (5.4)

For anti-clockwise rotation: $T_e^* \leq T_e \leq (T_e^* + \Delta T)$ (5.5)

where T_e is the actual torque developed, T_e^* is the reference torque, and ΔT is the torque band. While implementing these equations under software control, (5.4) and (5.5) are interpreted as follows:

If $(T_e^* - T_e) \geq \Delta T$, $T_{st} = 1$

If $\Delta T > (T_e^* - T_e) \geq 0$ & $T_{st} = 0$, $T_{st} = 0$

If $\Delta T > (T_e^* - T_e) \geq 0$ & $T_{st} = 1$, $T_{st} = 1$

If $(T_e^* - T_e) \leq -\Delta T$, $T_{st} = -1$

If $-\Delta T < (T_e^* - T_e) \leq 0$ & $T_{st} = 0$, $T_{st} = 0$

If $-\Delta T < (T_e^* - T_e) \leq 0$ & $T_{st} = -1$, $T_{st} = -1$

where T_{st} is status of torque.

Torque status '1' means actual torque less than the lower limit of torque reference and hence the torque needs to be increased. Torque status '-1' means the actual torque is more than the upper limit of torque reference and a reduction of the torque is necessary. Both torque status '-1' and '1' require active voltage vectors. Torque status '0' means the actual torque need not change and it requires zero vectors.

The optimum switching table is shown in Table.5.1 [48]. This table represents the operation of different active and zero vectors in different sectors based upon the flux status (ψ_{st}) and torque status (T_{st}). There are six sectors here similar to the sectors shown in Fig. 3.5 in Chapter 3. The voltage vector changes at the beginning of every sector and each sector is equal to an interval of $\pi/3$ radian.

Table. 5.1

		Sector-I	Sector-II	Sector-III	Sector-IV	Sector-V	Sector-VI
$\psi_{st}=0$	$T_{st}=1$	$V_s(1,1,0)$	$V_s(0,1,0)$	$V_s(0,1,1)$	$V_s(0,1,1)$	$V_s(1,0,1)$	$V_s(1,0,0)$
	$T_{st}=0$	$V_s(1,1,1)$	$V_s(0,0,0)$	$V_s(1,1,1)$	$V_s(0,0,0)$	$V_s(1,1,1)$	$V_s(0,0,0)$
	$T_{st}=-1$	$V_s(1,0,1)$	$V_s(1,0,0)$	$V_s(1,1,0)$	$V_s(0,1,0)$	$V_s(0,1,1)$	$V_s(0,0,1)$
$\psi_{st}=1$	$T_{st}=1$	$V_s(0,1,0)$	$V_s(0,1,1)$	$V_s(0,1,1)$	$V_s(1,0,1)$	$V_s(1,0,0)$	$V_s(1,1,0)$
	$T_{st}=0$	$V_s(0,0,0)$	$V_s(1,1,1)$	$V_s(0,0,0)$	$V_s(1,1,1)$	$V_s(1,0,0)$	$V_s(0,0,0)$
	$T_{st}=-1$	$V_s(0,0,1)$	$V_s(1,0,1)$	$V_s(1,0,0)$	$V_s(1,1,0)$	$V_s(0,1,1)$	$V_s(0,1,1)$

5.3 Quasi-Resonant Inverter-fed Induction Motor Drive

A quasi-resonant inverter as shown in Fig. 5.2 is operated under the DTC scheme with soft-switching operation for both link and inverter switching devices. The topology of the quasi-resonant dc link three-phase inverter is the same as discussed in Chapter 4 (Fig. 4.3). The control strategy adopted in Chapter 4 to implement soft-switching of inverter devices has been based on modified space vector modulation (MSVM). In MSVM, the voltage vectors are operated in a particular repetitive sequence such as vectors V_1 to V_6. However, in case of the DTC scheme, the voltage vectors do not operate sequentially. They follow a random pattern based on error of flux and torque. The same is true in the case of soft-switching inverter-fed induction motor drive under the DTC scheme. Therefore, a control strategy needs to be developed based on non-sequential operation of voltage vectors.

The principle of operation of switching devices in the quasi-resonant dc link and the inverter for the DTC scheme is the same as discussed in section 4.2 in Chapter 4. After knowing the flux

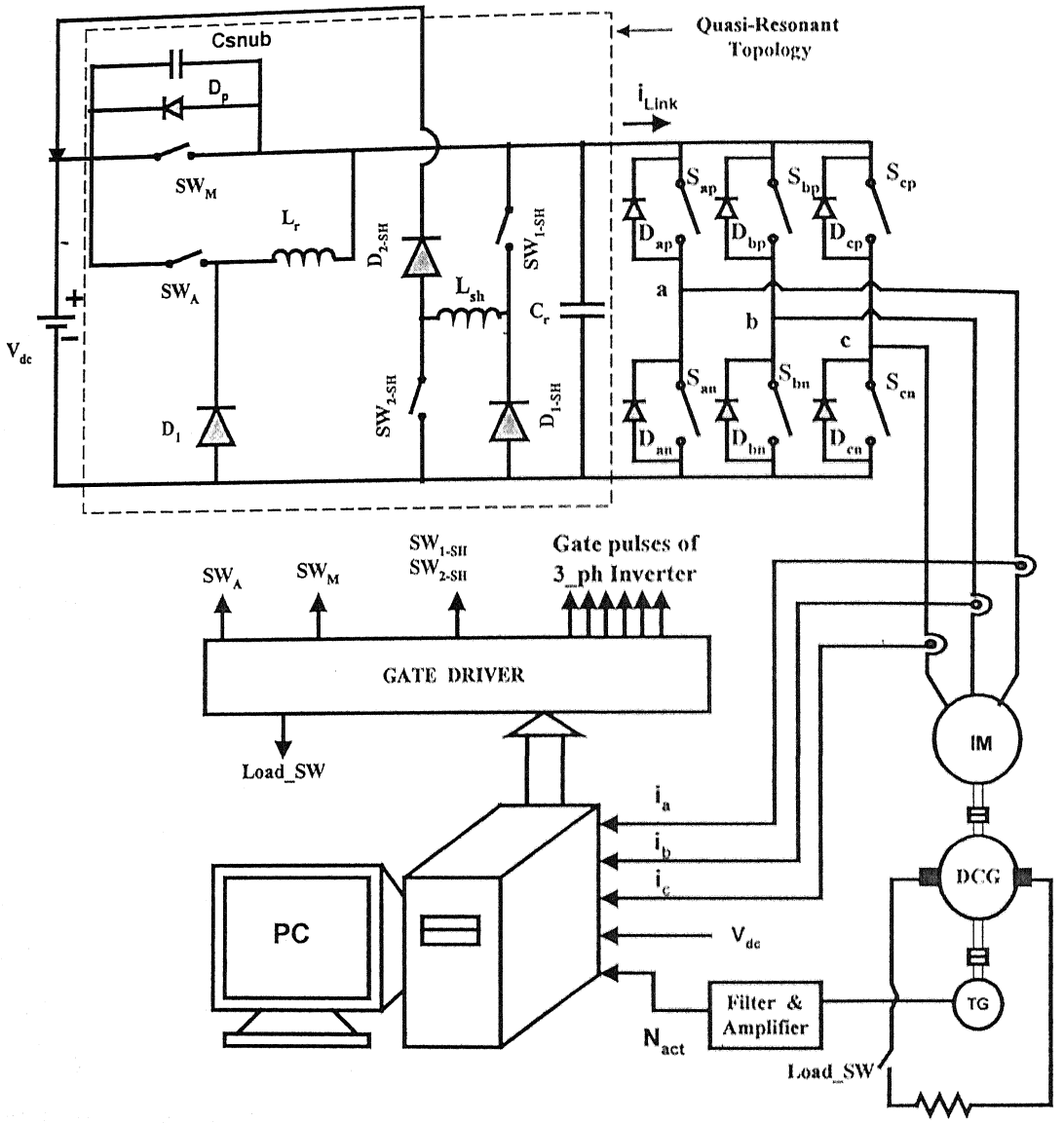


Fig.5.2. Quasi-resonant inverter-fed DTC Scheme for an induction motor drive.

status and torque status, the desired incoming voltage vector (active or zero) is picked up from the optimum switching vector table as shown in Table 5.1. This voltage vector represents the switching status of devices in the inverter to be operated in a subsequent step while the status of the earlier voltage vector (known as outgoing voltage vector) differs from the incoming voltage

vector. The switching strategy for the devices in the resonant link and inverter between any two different voltage vectors (incoming and outgoing vectors) is shown in Fig. 5.3. This strategy can be applied independent of whether the voltage vectors operate sequentially or randomly.

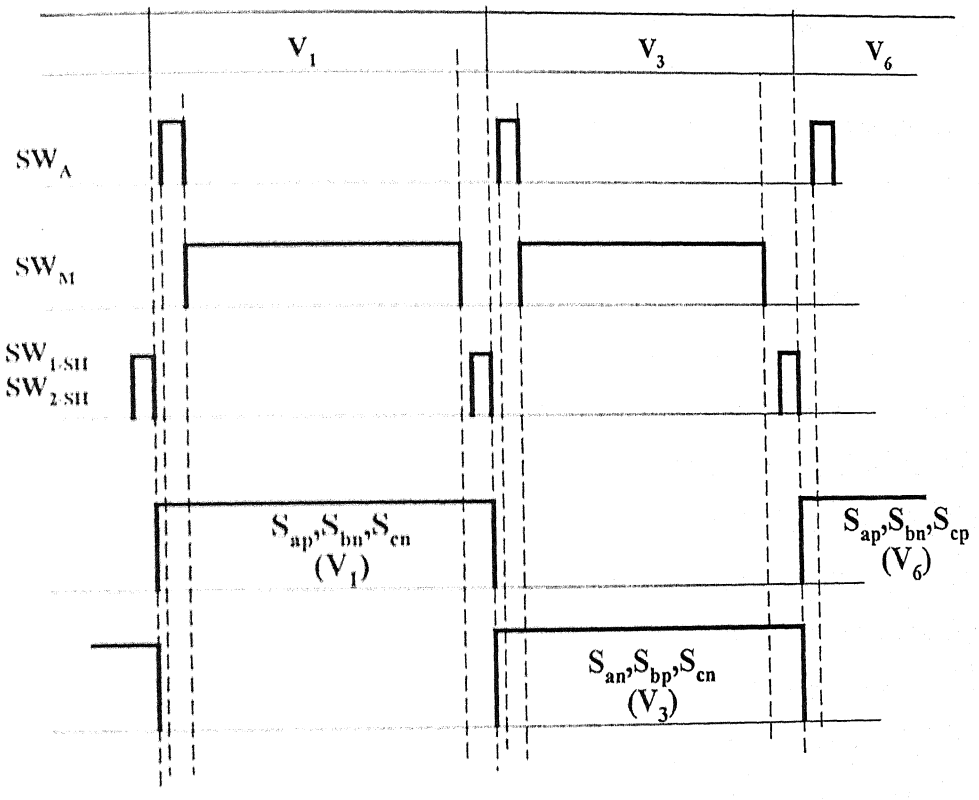


Fig. 5.3. Controlling operation for switches in quasi-resonant link inverter

To enable an incoming voltage vector and disable an outgoing vector, certain steps, as given below, are to be followed.

(i) Gate pulses from the main switch SW_M and the auxiliary switch SW_A in the link

are withdrawn.

(ii) Gate pulses to the shunt switches $SW_{1\text{-}SH}$ and $SW_{2\text{-}SH}$ are released independent of direction of the dc link current.

(iii) After the resonant capacitor C_r discharges to zero, the status of inverter switches is changed by disabling outgoing voltage vector and enabling incoming voltage vector.

(iv) The shunt switches are turned off.

(v) The auxiliary switch is turned on for a small interval.

(vi) As the voltage of dc link attains the source voltage, the main switch SW_M is turned on while the auxiliary switch SW_A is turned off.

5.4 Control Strategy

The flow-chart for the control strategy of soft-switched inverter-based DTC scheme is shown in Appendix-E. In the quasi-resonant topology, the shunt-switches ($SW_{1\text{-}SH}$, $SW_{2\text{-}SH}$) play a crucial role by ensuring ZVS operation during bi-directional flow of link current, while the main switch SW_M and the auxiliary switch SW_A are used to disrupt/energize the resonant dc link from the input supply. This flow-chart in Appendix-E formulates co-ordination among switches in the quasi-resonant link (SW_M, SW_A, $SW_{1\text{-}SH}$ and $SW_{2\text{-}SH}$) and the inverter during soft-switching operation. It is to be noted that the soft-switching of all devices in the quasi-resonant inverter must be ensured when the voltage vectors are operated randomly.

Once the status of the incoming voltage vector is known from the optimum switching vector table, it is compared with the outgoing one that has already been latched. If it is found that both incoming and outgoing voltage vectors are the same, then there is obviously no need to disable the outgoing voltage vector. This means that the status of switches in the quasi-resonant dc link and the inverter will remain unchanged. On the other hand, if the incoming voltage vector differs from the outgoing one, the soft-switching steps as explained in the earlier section are adopted.

5.4.1 Operation during the Regenerative Mode:

In case of the conventional DTC as shown in Fig. 5.1, when the reference speed command is reversed, the reference torque and torque error also reverse. As a result, the torque status is changed to negative. The status of flux remains the same. Considering the status of torque and stator flux, appropriate voltage vectors are picked up from the optimum switching vector table. This leads to a gradual reduction of frequency of the applied voltage to the motor resulting in negative torque. Therefore, rotor starts decelerating, thereby regenerating power from the drive system to supply source. The average dc link current becomes negative and it flows from inverter to source. This will continue till the rotor speed becomes zero. As the motor speed approaches zero, the applied voltage phase sequence is automatically changed and motor accelerates in the negative direction till the reference speed (reverse motoring) is attained. In case of QRDCL inverter-fed DTC scheme, transitions from outgoing to incoming voltage vectors need to be handled in such a way that soft-switching of all switching devices is ensured during rotor speed variation from the reference speed to zero. The switching sequences of inverter and resonant link devices are programmed for soft-switching by software control shown in the flow-chart of Appendix-E. During regenerative mode, the anti-parallel diode D_p remains forward-biased due to negative link current. The gating pulse to the main switch SW_M is present, but the device does not conduct. The auxiliary switch is in the off state. When soft-switching of inverter devices is desired, the gating pulse to SW_M is withdrawn and the shunt switches ($SW_{1\text{-}SH}$ and $SW_{2\text{-}SH}$) are activated by releasing the gate pulses. The link current gradually shifts from diode D_p to the inductor L_{sh} in series with shunt switches. As long as the diode D_p conducts, the dc link is clamped to the source voltage. When the current in D_p becomes zero, the dc link is disconnected from the source and the dc link current is transferred to the shunt inductor L_{sh}. At this instant, the resonant capacitor C_r across the dc link starts discharging. As the capacitor C_r discharges to zero, the outgoing voltage vector is disabled and the incoming voltage vector is enabled by switching off and on of appropriate inverter switches. Soft-switching of inverter devices with ZVS is achieved by this process. The shunt-switches are turned off following this operation under ZVS due to resonant capacitor. The dc link current now flows through the resonant capacitor charging it up from zero to source voltage. When the voltage across the resonant capacitor is equal to the

source voltage, the diode D_p becomes forward-biased. The switches SW_A and SW_M are enabled as shown in Fig. 5.3 to complete one switching cycle corresponding to outgoing and incoming voltage vectors under soft-switching. Although switches SW_A and SW_M do not conduct during the regenerative mode, they may conduct in the motoring mode. Therefore, switching pulses are required as the control scheme functions independent of the direction of the dc link current.

5.5 Implementation

The implementation of quasi-resonant DTC scheme is shown in Fig. 5.2. The implementation is through both software and hardware. The software implementation of the soft-switched DTC scheme is shown in Appendix-E. The hardware section comprises of IGBT drivers (i.e., for both quasi-resonant link and inverter), current sensors, voltage sensor, and a tacho-generator coupled with an induction motor-dc generator set. The dc generator is used for loading the induction motor. The output of the tacho-generator is filtered and buffered before connecting to the data-acquisition card. The data-acquisition card (ACL- 8112 PG) used is the same as used in section-4.5 of Chapter 4. The current and voltage sensors are of LEM type and their details are given in Appendix-B. The connections of all these sensors are shown in Fig. 5.2. The sensors measure various variables, such as currents, voltage, and speed and thus produce analog outputs which are fed to a high-speed 12-bit analog-to-digital converter (ADC) available on ACL-8112 PG. The data available in digital forms after AD conversion are the values of three-phase motor currents, dc link voltage and speed, which are further processed in the computer to determine the torque, stator flux, and status of the sector. These data along with the speed information are further taken to their respective comparators (speed, torque, flux) so as to generate the status of flux and torque that act as inputs to the optimum switching vector table (OSVT). The OSVT provides information of incoming voltage vectors from which the control strategy is carried out logically as explained in section 5.3. The switching status of inverter devices as well as those of resonant link is taken out digitally from two 8-bit output port of data acquisition card separately. These signals are further fed to high-speed opto-isolators (IC 6N137 given in Appendix-C) to generate gate signals for IGBTs. The complex part of implementation requiring real time computations is

performed by PC-based software. The loading of induction motor is implemented by an electronically controlled (MOSFET) switch connected in series with a rheostat and armature of the dc generator as shown in Fig. 5.2. The gate signal for this device is taken out through digital output port of the data acquisition card. The closure of MOSFET-based load switch is software-controlled and the time interval of loading is programmed through software. The sampling time for the real time control of the drive system is 185 μs.

5.6 Simulation and Experimental Results

The mathematical model is developed for the soft-switched DTC scheme and the complete system is analyzed using SABER simulator. The input dc voltage is 120 V. The values of resonant components are L_r = 8 μH, L_{sh} = 6 μH and C_r = 20 nF. The simulation is carried out to observe various responses for step-change in speed and load torque under soft-switching operation. Initially, soft-switching of inverter devices is studied from the gate pulses of the main switch and shunt-switches, and the corresponding dc link voltage. Soft-switching is ensured by observing zero dc link voltage when the shunt-switches are turned on. Figs. 5.4 - 5.9 show some typical simulation results.

Figure 5.4 shows the responses of speed, torque and flux for step change in reference speed from 0 to 500 rpm. After the steady state is reached, load torque change of 1 N-m for a small interval is initiated to observe the responses. It is noted that both stator flux and rotor speed are unaffected by the load torque change. The simulation results in Figs. 5.5 and 5.6 show the d- and q-axis quantities for fluxes and currents in stationary reference frame during the step change in reference speed and load torque. The expanded steady-state d-q currents and fluxes are shown in Figs. 5.7 and 5.8 respectively. Figure 5.9 shows responses of stator flux and d-q axis currents during speed reversal in the forward and reverse directions. It may be noted that there are notches in the stator flux during speed reversal. This may be attributed to high stator resistance of the motor. The notches disappear when the stator resistance is of a small value.

The experimental setup is shown in Fig. 5.2. The turn-on and turn-off transitions of inverter

switches are achieved under ZVS conditions. ZVS operation is possible after the dc link voltage is made zero. Figure 5.10 shows waveforms of gate pulses for auxiliary (SW_A), main (SW_M), shunt switches (SW_{1SH}, SW_{2SH}), and link voltage for both simulation and experiment. The switching sequence of dc link switches sets the link voltage zero for soft-switching of devices independent of the direction of the link current as may be clearly seen from Fig. 5.10 both under simulation and experiment. The simulation and experimental d-q axis fluxes are shown in 5.11. The experimental waveforms match quite well with simulation results. The responses of speed and stator flux from both simulation and experiment during a step change in reference input speed command (0-500 rpm) are shown in Fig. 5.12. The stator flux attains the reference command value much faster than the speed. The experimental responses of flux and speed during a load torque change are shown in Figs. 5.13 and 5.14 respectively. The instants of switching of load are controlled electronically by a MOSFET switch as shown in Fig. 5.2. The switch is connected in series with armature of a dc generator coupled with the induction motor. G_{load} is the gate pulse to the MOSFET switch. It is observed that the stator flux and motor speed remain unaffected by application of load torque. The experimental d- and q-axis currents for step change in reference speed are shown in Fig. 5.15. The response of speed with step change in reference speed command in both directions is shown in Fig. 5.16. It is observed that the stator flux remains unaffected during the four-quadrant operation.

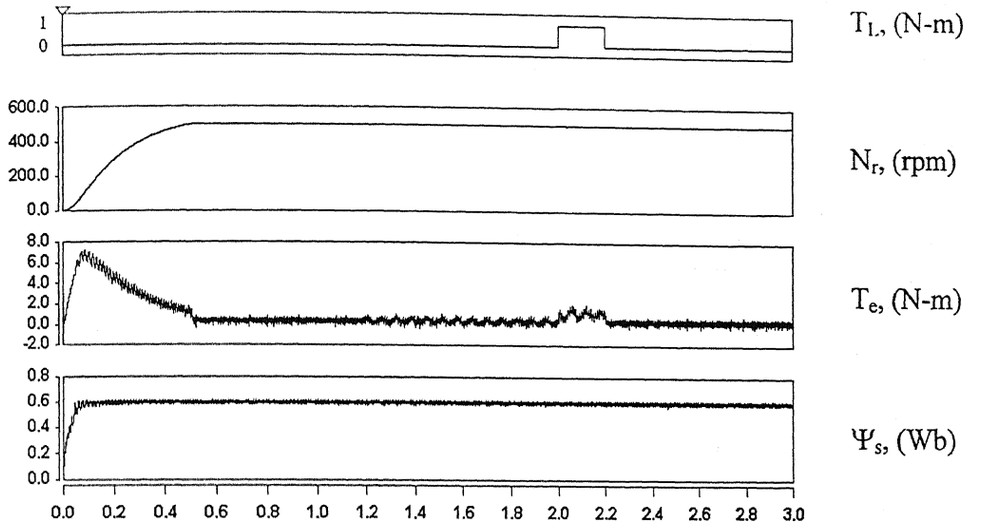


Fig. 5.4. Transient responses of speed (N_r), torque developed (T_e), and stator flux (Ψ_s) during step change in reference speed (i.e., 0-500 rpm) and step change in load torque (T_L) of 1 N-m.

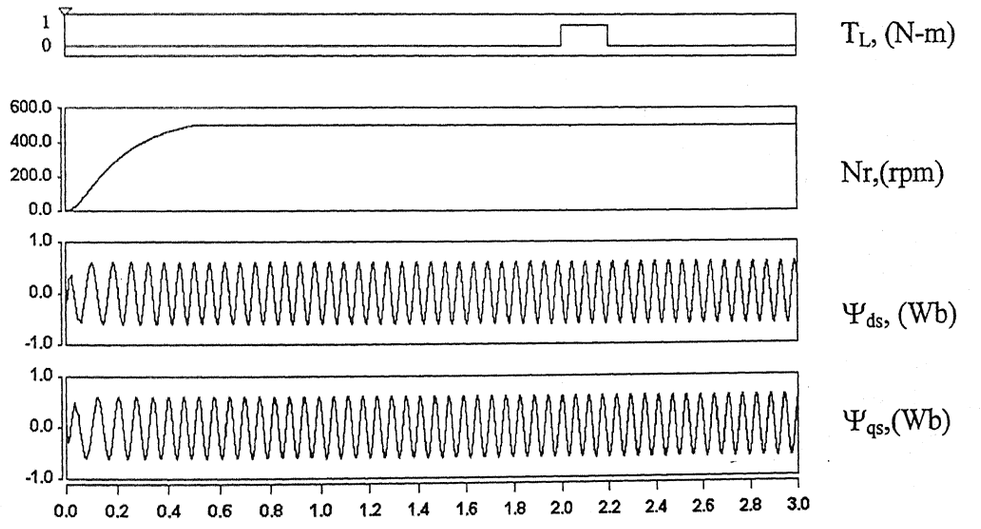


Fig.5.5. Transient responses of speed (Nr), d-q-axis stator flux (Ψ_{ds}, Ψ_{qs}) during step change in reference speed (i.e., 0-500 rpm) and step change in load torque of 1 N-m.

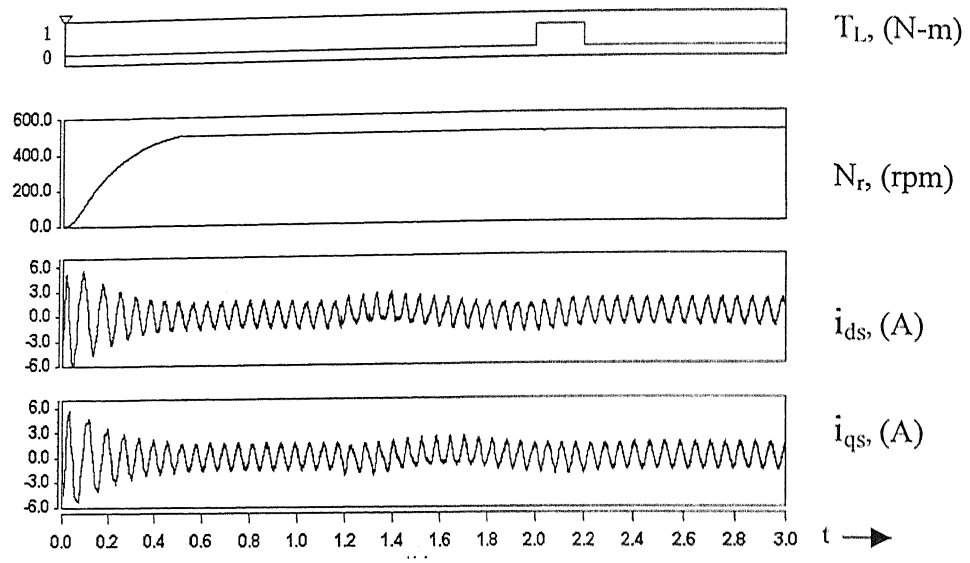


Fig. 5.6. Transient responses of speed (Nr), d-q axis stator currents (i_{ds}, i_{qs}) during step change in reference speed (i.e., 0-500 rpm) and step change in load torque of 1 N-m.

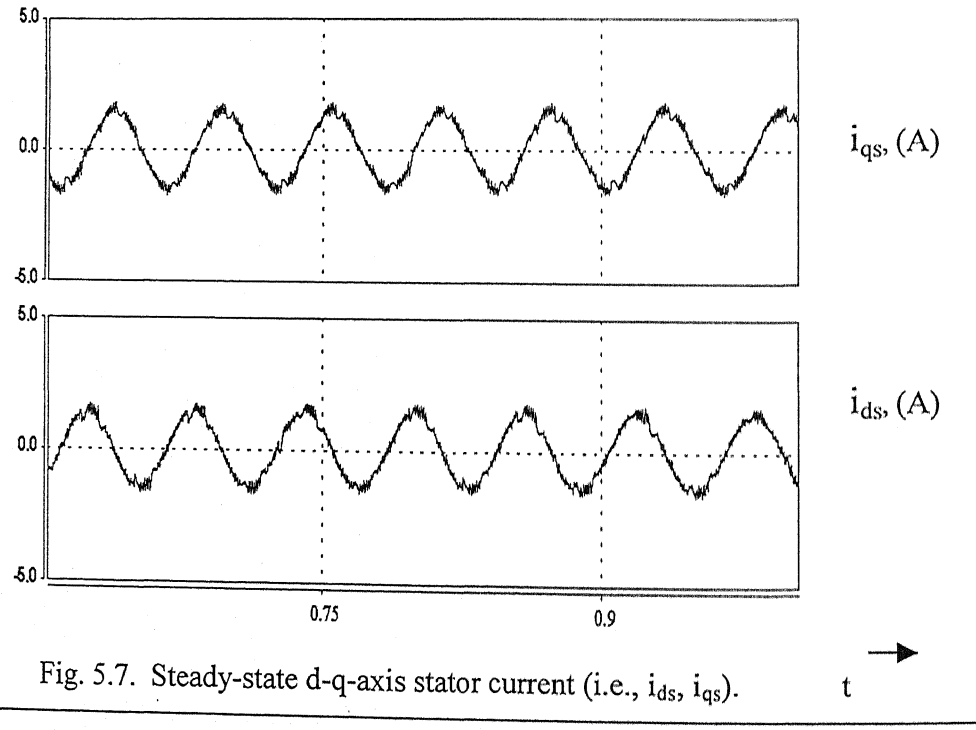


Fig. 5.7. Steady-state d-q-axis stator current (i.e., i_{ds}, i_{qs}).

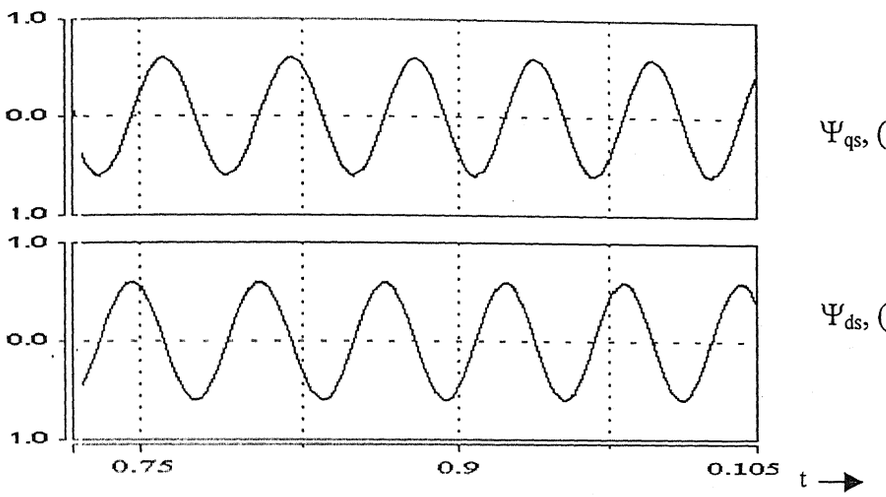


Fig. 5.8. Steady-state d-q-axis of stator fluxes (i.e., Ψ_{ds}, Ψ_{qs})

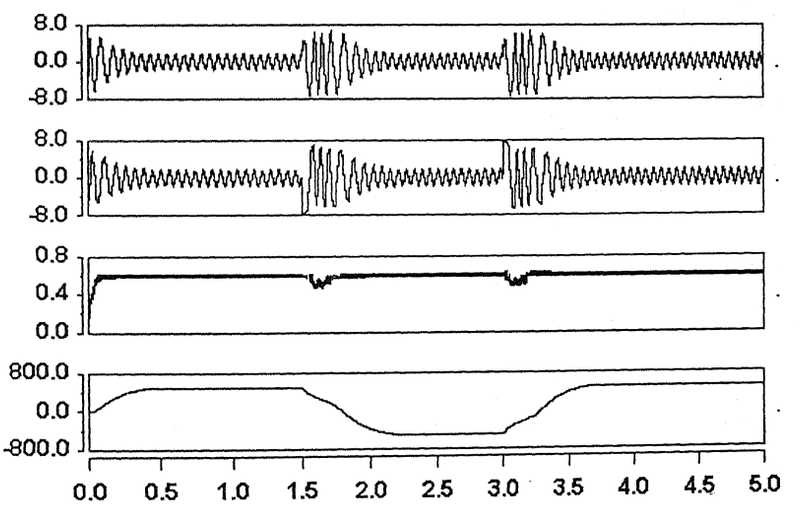
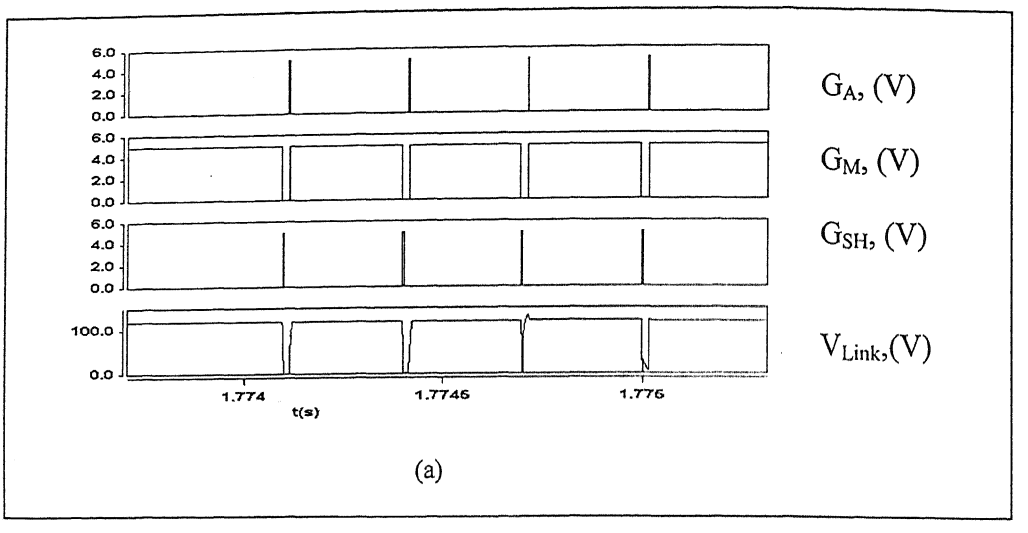


Fig.5.9. Responses of rotor speed, stator flux, and d-q-axis stator current



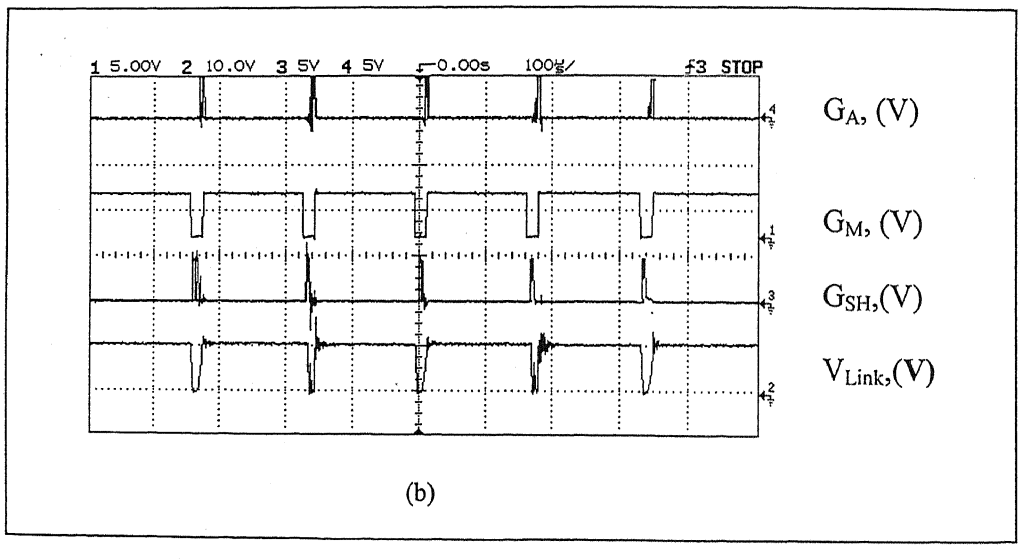
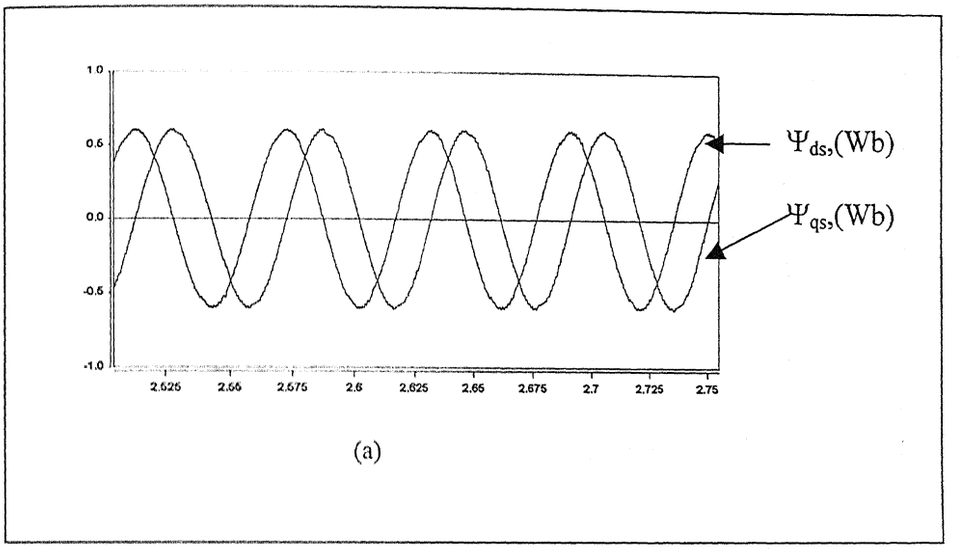
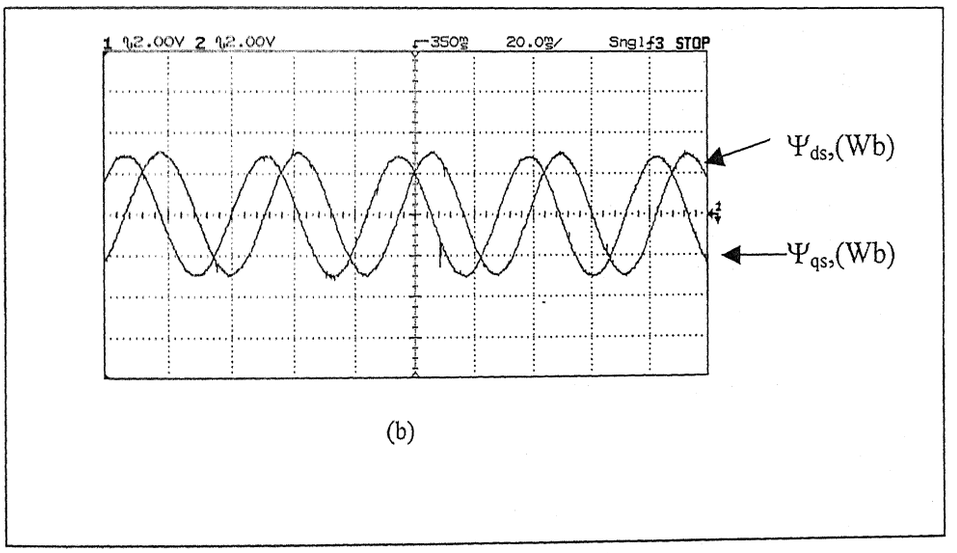


Fig. 5.10. G_A, G_M, G_{SH} Gate pulses of switches SW_A, SW_M, and (SW_{1SH}, $SW_{2\text{-}SH}$).
V_{Link}: Dc link voltage (scale of V_{Link} in experimental - 1:10)
(a) Simulation (b) Experimental

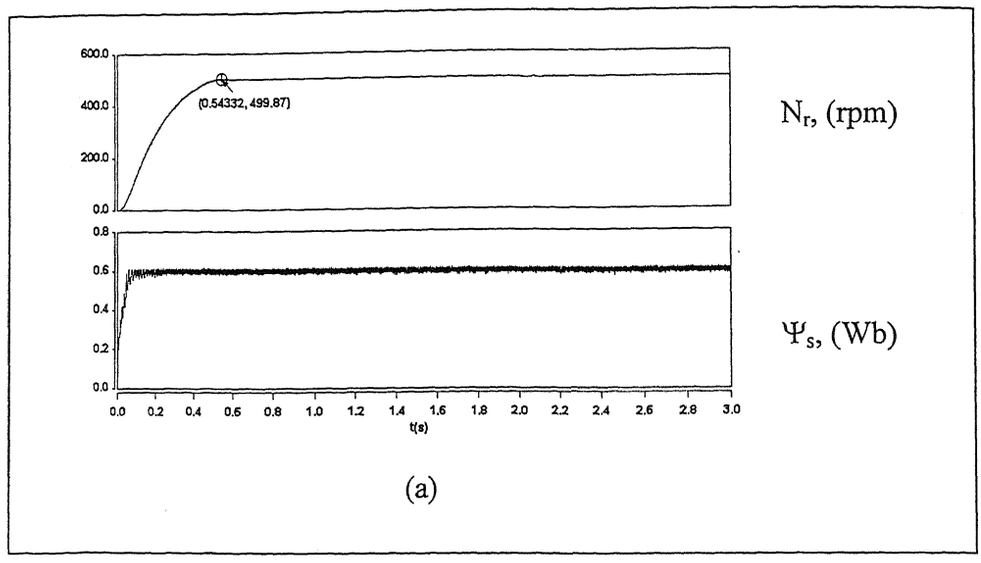


(a)



(b)

Fig. 5.11. The d-axis and q-axis stator fluxes
(a) Simulation
(b) Experimental (Scale : 5V/Wb)



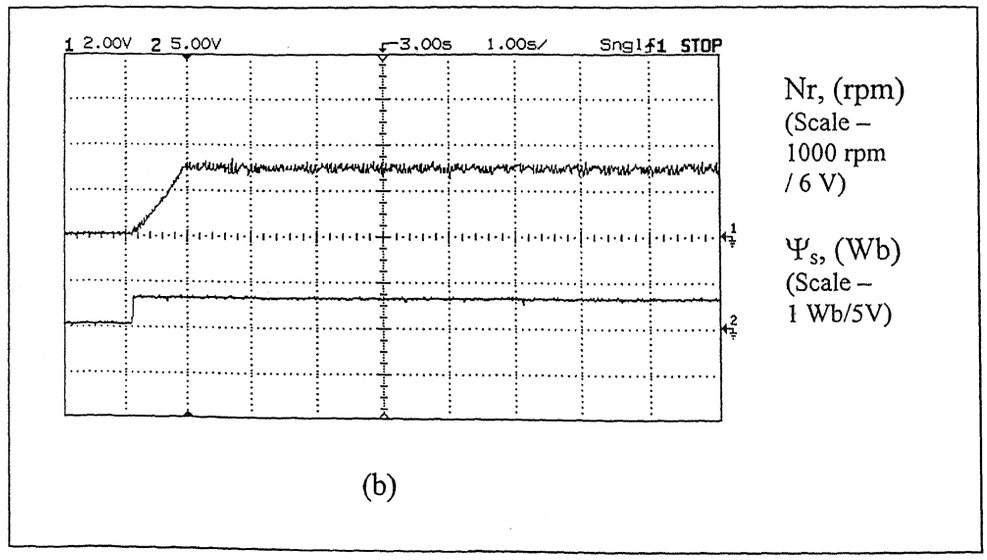
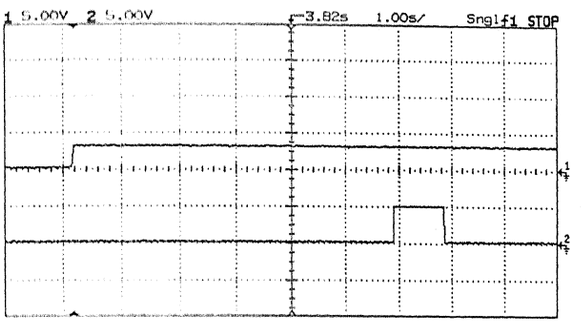


Fig. 5.12. Transient responses of speed (N_r) and stator fluxes (Ψ_s) during step change in reference speed (i.e., 0 – 500 rpm) and reference stator flux 0.6 Wb

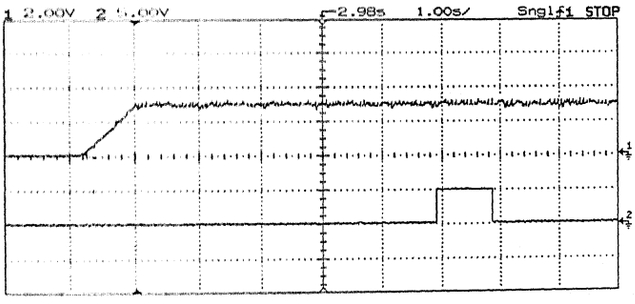
(a) Simulation (b) Experimental



Ψ_s, (Wb)
(Scale:
1000 rpm
/ 6 V)

G_{load},
(V)

Fig. 5.13. Flux (Ψ_s) responses during step change in reference speed from 0 to 500 rpm and a load torque of 1 N-m is applied by closing load switch for 1 sec.
(G_{Load} – gate pulse of load switch)



Nr, (rpm)
(Scale:
1000 rpm
/ 6 V)

G_{load},
(V)

Fig.5.14. Speed (N_r) responses during step change in reference speed from 0 to 500 rpm and a load torque of 1 N-m is applied by closing load switch for 1 sec.
(G_{Load} – gate pulse of load switch)

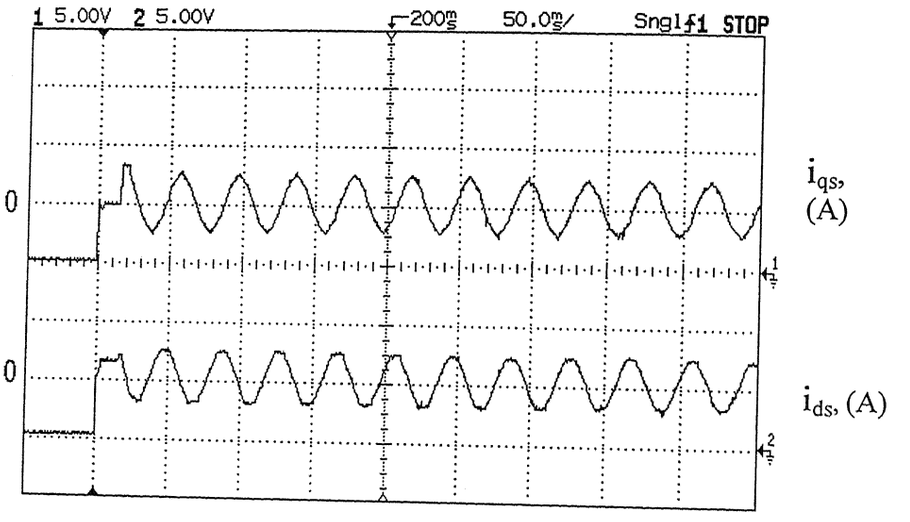


Fig. 5.15. i_{ds}, i_{qs} : d-q –axis currents of stator during step change in reference speed from 0 to 500 rpm. (scale : 2 mp/volt)

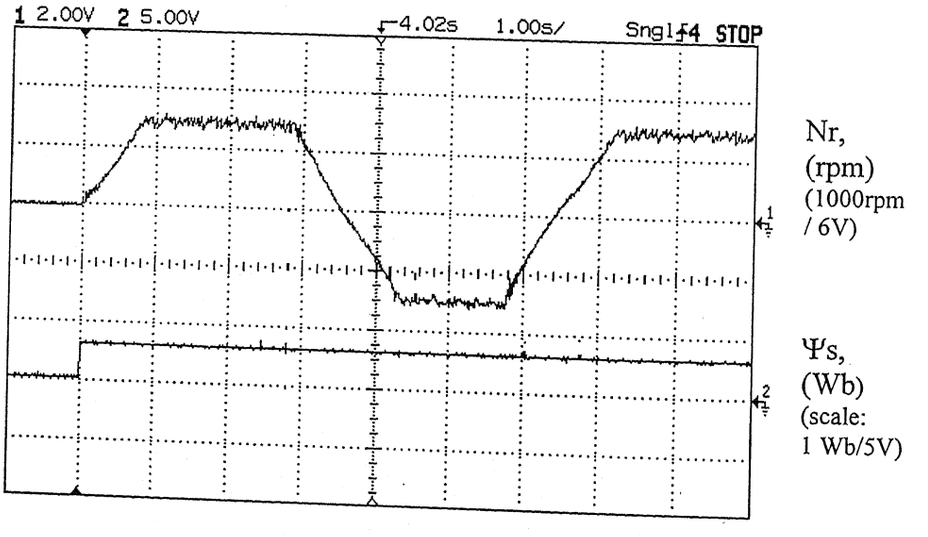


Fig. 5.16 Responses of rotor speed (N_r) and flux (Ψ_s) during speed reversal in reference input

5.7 Reduced order Robust Stator Flux Observer for Direct Torque Controlled Induction Motor Drive fed from Quasi-Resonant Inverter.

The foremost requirement for a flux-feedback type vector control is accurate information regarding the relevant flux vector of the motor. Since direct measurement using intrusive flux sensors calls for a special design or a major modification of the motor, the calculation of motor fluxes from terminal quantities employing motor parameters has been of great interest for long time. The estimation of rotor fluxes of an induction motor using observers has been attempted in the past by researchers [56-58]. In many of these cases, the observer was used in closed-loop as described in [55], where the rate of convergence can be suitably adjusted depending on system poles to have satisfactory performance. On the contrary, open-loop observers [55, 56] simulate the motor states without any prediction error feedback and thus the rate of convergence is solely dependent on the motor parameters [58].

In conventional field-oriented control and direct torque control (DTC), the flux estimators are open-loop real-time simulations of machine equations without feedback of any corrective prediction error. The use of feedback of corrective prediction error not only speeds up convergence of flux estimates, but also reduces the sensitivity of the estimates to parameter variations [56]. The flux estimates provided by observer theory [56] are classified according to the following categories:

- Full-order observer (referred to stator / rotor)
- Reduced-order observer (referred to stator / rotor)

In both of these schemes, the estimation technique can be applied to different variables such as speed, current, and flux. In [52], an adaptive flux observer was reported for a speed-sensorless direct torque control of induction motors. A reduced-order stator-flux observer [53, 54] was presented for a vector-controlled cycloconverter-fed synchronous motor drive.

In this section, a reduced-order robust stator flux observer is developed for a direct torque controlled induction motor drive fed from a quasi-resonant inverter. This observer is analyzed by SABER simulator and the simulation results are compared with the results from the experimental setup to validate the scheme.

5.7.1 Development of the Reduced Order Observer from IM Model:

The induction motor in a stationary reference frame is represented by the following state equations.

$$\begin{bmatrix} \dot{\Psi}_{qs} \\ \dot{\Psi}_{ds} \\ \dot{i}_{qs} \\ \dot{i}_{ds} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -r_s & 0 \\ 0 & 0 & 0 & -r_s \\ r_r/\sigma L_s L_r & -w_r/\sigma L_s & -(r_s+r_r)/\sigma L_s & w_r \\ w_r/\sigma L_s & r_r/\sigma L_s L_r & -w_r & -(r_s+r_r)/\sigma L_s \end{bmatrix} \begin{bmatrix} \Psi_{qs} \\ \Psi_{ds} \\ i_{qs} \\ i_{ds} \end{bmatrix}$$

$$+ \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1/\sigma L_s & 0 & 0 & 0 \\ 0 & 1/\sigma L_s & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{qs} \\ v_{ds} \\ 0 \\ 0 \end{bmatrix} \qquad (5.6)$$

The above equation is of the form

$$\dot{X} = [A]X + [B]U$$

where $\sigma = 1 - L_m^2/(L_s L_r)$

Equation (5.6) can be written as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u$$

$$y = [x_2] \qquad (5.7)$$

where

$x_1 = [\Psi_{qs}, \Psi_{ds}]^T$, $x_2 = [i_{qs}, i_{ds}]^T$, $u = [v_{qs}, v_{ds}]^T$

$$A_{11} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \quad A_{12} = \begin{bmatrix} -r_s & 0 \\ 0 & -r_s \end{bmatrix} \quad A_{21} = \begin{bmatrix} r_r/\sigma L_s L_r & -w_r/\sigma L_s \\ w_r/\sigma L_s & r_r/\sigma L_s L_r \end{bmatrix}$$

$$A_{22} = \begin{bmatrix} -(r_s+r_r)/\sigma L_s & w_r \\ w_r & -(r_s+r_r)/\sigma L_s \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad B_2 = \begin{bmatrix} 1/\sigma L_s & 0 \\ 0 & 1/\sigma L_s \end{bmatrix}$$

5.7.2 Observer Design:

Equation (5.7) yields

$$\dot{x}_1 = A_{11}x_1 + A_{12}x_2 + B_1 u$$
$$\dot{x}_2 = A_{21}x_1 + A_{22}x_2 + B_2 u \tag{5.8}$$

The state vector is not available for measurement and needs to be estimated by the observer. The vector x_2 can be measured using current sensors and is available as output y. If the estimated state 'x_1' is denoted '$\hat{x}_1$', then using a gain matrix K of dimension (2×2) for a reduced-order flux observer, the observer equation can be written as follows:

$$\dot{\hat{x}}_1 = A_{11}\hat{x}_1 + A_{12}x_2 + B_1 u - K(\dot{y} - \dot{\hat{y}})$$
$$\dot{\hat{x}}_1 = A_{11}\hat{x}_1 + A_{12}x_2 + B_1 u - K(\dot{x}_2 - A_{21}\hat{x}_1 - A_{22}x_2 - B_2 u)$$
$$= A_{11}\hat{x}_1 + A_{12}x_2 + B_1 u + KA_{21}(\hat{x}_1 - x_1) \tag{5.9}$$

The estimated state error equation is obtained from (5.8) and (5.9), and is given by

$$\dot{\tilde{x}}_1 = \dot{\hat{x}}_1 - \dot{x}_1 = (A_{11} + KA_{21})(\hat{x}_1 - x_1) = (A_{11} + KA_{21})\,\tilde{x}_1 \tag{5.10}$$

where $\tilde{x}_1 = \hat{x}_1 - x_1$

It is desirable that the estimated state '$\hat{x}_1$' should follow the actual state 'x_1' closely with a good dynamic response. This necessitates the eigenvalues of $(A_{11}+ KA_{21})$ to have negative real parts. The matrix pair (A_{11}, A_{21}) is found to be observable for all values of w_r. Hence, the eigenvalues of the matrix $(A_{11}+ KA_{21})$ can be suitably assigned in the left half of s-plane so that the estimated state $\hat{x}_1$ approaches the actual state x_1 asymptotically.

The estimate of the state vector x_1 with a prediction error feedback assumes the form

$$\dot{\hat{x}}_1 = A_{11}\hat{x}_1 + A_{12}x_2 + B_1 u + K[\dot{\hat{y}} - \dot{y}]$$
$$= A_{11}\hat{x}_1 + A_{12}x_2 + B_1 u + K[A_{21}\hat{x}_1 + A_{22}x_2 + B_2 u - \dot{y}]$$
$$= (A_{11} + KA_{21})\hat{x}_1 + (A_{12} + KA_{22})x_2 + (B_1 + KB_2)\,u - K\dot{y} \tag{5.11}$$

The above observer given by (5.11) contains a derivative term ($\dot{y}$), which is unacceptable as it amplifies the noise due to quantization, measurement or otherwise. Hence, a substitution by a dummy state variable is used to eliminate the derivative term as follows:

$$z = \hat{x}_1 + Ky \tag{5.12}$$

where $z = [z_1,\ z_2]^T$

The final observer equation obtained from (5.11) and (5.12) is given by

$$\begin{aligned}\dot{z} &= (A_{11} + KA_{21})\hat{x}_1 + (A_{12} + KA_{22})x_2 + (B_1 + KB_2)u \\ &= (A_{11} + KA_{21})(z - Ky) + (A_{12} + KA_{22})x_2 + (B_1 + KB_2)u \\ &= (A_{11} + KA_{21})z + [(A_{12} + KA_{22}) - (A_{11} + KA_{21})K]y + (B_1 + KB_2)u \end{aligned} \tag{5.13}$$

The estimated state can be obtained from the dummy state variable, z, as follows:

$$\hat{x}_1 = z - Ky \tag{5.14}$$

5.7.3 Gain Setting of the Observer:

For the motor parameters given in Appendix-C, the characteristic equation of (5.10), which gives the estimated state error dynamics, is given by

$$\det [sI - (A_{11} + KA_{21})] =$$

$$= \det\left\{ s\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix} - \begin{bmatrix}k_{11} & k_{12}\\ k_{21} & k_{22}\end{bmatrix}\begin{bmatrix}212.15 & -19.87w_r\\ 19.87w_r & 212.15\end{bmatrix}\right\} = 0 \tag{5.15}$$

where 'A_{11}' is a null matrix and $K = \begin{bmatrix}k_{11} & k_{12}\\ k_{21} & k_{22}\end{bmatrix}$, is the gain matrix of the observer.

The aim is to design a reduced order observer robust to speed variation in the operating speed range. This necessitates the observer dynamics to be largely insensitive to motor speed. To make the error dynamics independent of w_r, (5.15) should have terms independent of w_r. However, it may not be possible to completely eliminate w_r terms in (5.15). Hence some of the elements of the given matrix are made zero to eliminate a few terms containing w_r in (5.15).

The following choice leads to a simple implementation of the observer gain matrix elements.

$k_{12}=0,\ k_{21} = 0,\ k_{11} = k_{22} = k$

So the characteristic equation (5.15) becomes

$$(s - 212.15\,k)^2 + (19.87\,k\,w_r)^2 = 0$$

$$s^2 - 424.3\,k\,s + 45007.0\,k^2 + 394.8\,w_r^2\,k^2 = 0 \tag{5.16}$$

The equation (5.16) is of the form

$$s^2 + p\,s + (w_r^2\,q + r) = 0 \tag{5.17}$$

where $p = -424.3\,k$, $q = 394.8\,k^2$, and $r = 45007.0\,k^2$

The roots of (5.17) are eigenvalues of the error equation. For the error to become zero asymptotically, the roots of (5.17) should have negative real parts. In order to have negative real parts of the roots of (5.17), the terms 'p' and '$(w_r^2\,q + r)$' should be positive. Hence 'k' can be easily selected to have $p > 0$ and $(w_r^2\,q + r) > 0$. Since $(w_r^2\,q)$ is the only variable in (5.17), the movement of the roots (eigenvalues) with speed (w_r) can be studied from the root locus of the transfer function

$$\frac{w_r^2\,q}{s^2 + p\,s + r} \tag{5.18}$$

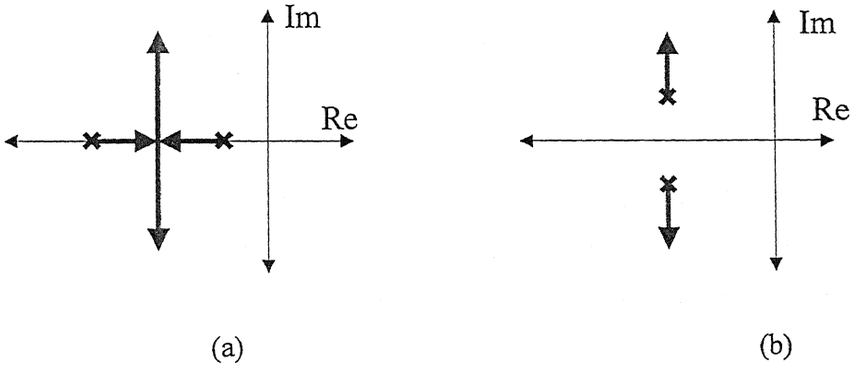


Fig. 5. 17: Root loci of the observer poles with variation of speed
(a) For real roots at $w_r = 0$ (b) For complex conjugate roots at $w_r = 0$

It can be observed from Fig. 5.17 that the root locus of (5.18) always remains in the left half of s-plane for variation in w_r. Hence it can be concluded that the system is stable for variation in w_r (robust to speed variation). Since $p = -423.3\,k$, to obtain a positive value of 'p', k should have a negative value.

$$k < 0 \tag{5.19}$$

It is also observed that input-coefficient matrix ($\boldsymbol{B}_1 + \boldsymbol{K}\boldsymbol{B}_2$) (i.e., for input **u**) in (5.13) is function of gain matrix ($\boldsymbol{K}$).

$$B_1 + KB_2 = \begin{bmatrix} 1+(k/\sigma L_s) & 0 \\ 0 & 1+(k/\sigma L_s) \end{bmatrix} \tag{5.20}$$

where $\boldsymbol{u} = [v_{qs}, v_{ds}]^T$

The diagonal elements of the input matrix of the observer ($\boldsymbol{B}_1 + \boldsymbol{KB}_2$) should be positive for stability. To impose this restriction $(1+k/\sigma L_s) > 0$.

Hence $k > -\sigma L_s$. (5.21)

From (5.19) and (5.21), the value of of 'k' in the observer gain matrix is obtained as follows:

$$(-\sigma L_s < k < 0) \Rightarrow (-0.05 < k < 0). \tag{5.22}$$

Thus, the gain matrix is $\boldsymbol{K} = \begin{bmatrix} k & 0 \\ 0 & k \end{bmatrix}$ where $(-0.05 < k < 0)$

5.8 Control Strategy and Implementation of Stator Flux Observer

The flow-chart of reduced order observer is given in Appendix- F which shows the procedure for step-by-step implementation. The implementation is partly software and partly hardware-based. The hardware section remains the same in both the cases (with and without observer). Only software needs to be modified to implement observer based DTC.

Initially, the elements of observer gain matrix (K) are decided based on (5.22). The sub-matrices A_{11}, A_{12}, A_{21}, A_{22}, B_1, B_2 and their elements are determined as given in (5.7). The observer equation (5.13) is then programmed as shown in the flow-chart of Appendix- F. The observer flux is determined based on equation (5.13) after sensing the phase currents. The data acquisition card used is ACL-8112 PG as in Chapter 4. The rest of the hardware is similar to that detailed in section 5.4.

5.9 Simulation and Experimental Results from Observer

The DTC scheme employing the reduced-order stator flux observer with soft-switched inverter is analyzed with SABER simulator. Figure 5.18 shows stator flux from the observer and

the mathematical model (actual flux). The stator flux from the observer $\Psi_{s\text{-}obs}$ closely approaches the stator flux $\Psi_{s\text{-}mod}$ obtained from the mathematical model (actual flux) of induction motor. This shows that the performance of the observer is satisfactory. Figure 5.19 shows the four-quadrant operation of the induction motor drive with the magnitude of absolute observer gain | k | equal to 0.01. Typical experimental results are presented in Figs. 5.20 and 5.21. Figure 5.20 shows speed and flux responses for two values of observer gain with step change in reference speed and speed reversal. It is found that the stator flux remains unchanged during step changes in speed indicating decoupling between the torque and the flux. Figure 5.20 also demonstrates the four-quadrant operation capability of the drive. Figure 5.21 shows the speed response to a step change in reference speed of 500 rpm. After the motor has attained a steady state speed of 500 rpm, the response of speed is studied by initiating a step change in load torque of 1 Nm for an interval of 4 sec. The speed remains at the set value following the torque change.

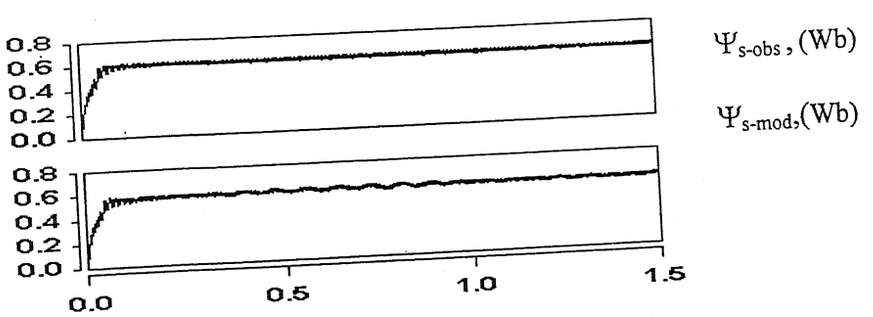


Fig. 5.18. Responses of stator fluxes from observer ($\Psi_{s\text{-}obs}$) and induction machine model ($\Psi_{s\text{-}mod}$) from SABER simulaton

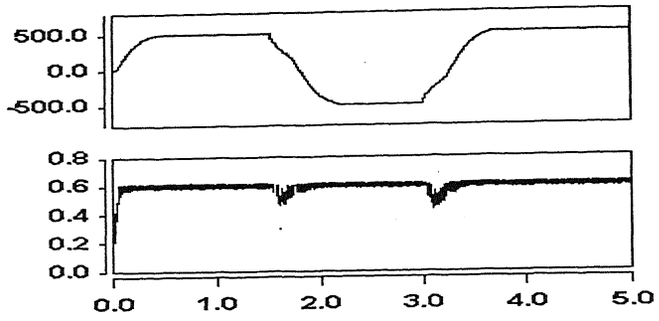
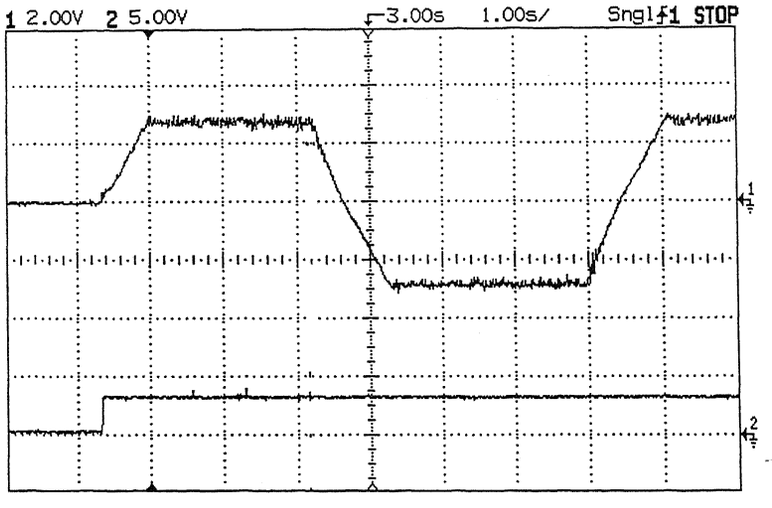
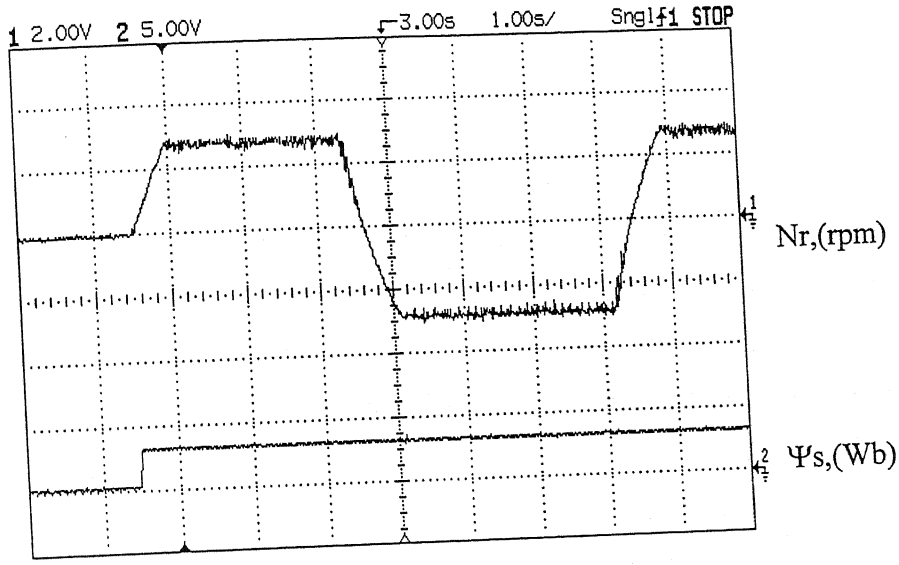


Fig. 5.19. Responses of rotor speed and flux for step change in reference speed command from SABER simulation.
Observer gain (k) = -0.01



(a) k = - 0.01

Fig. 5.20 Contd.



(b) k = -0.02

Fig. 5.20. Responses of rotor speed (Nr) and flux (Ψs) during speed reversal at different observer gains.
(a) k= -0.01 (b) k = -0.02.
(scale : 1000 rpm/ 6V for Nr and 1 Wb/ 5V for Ψs

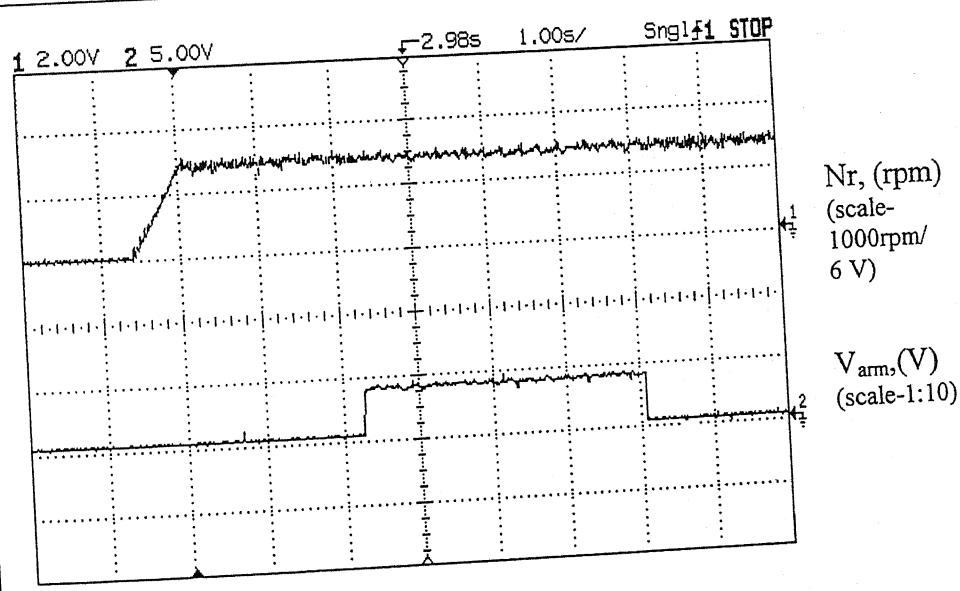


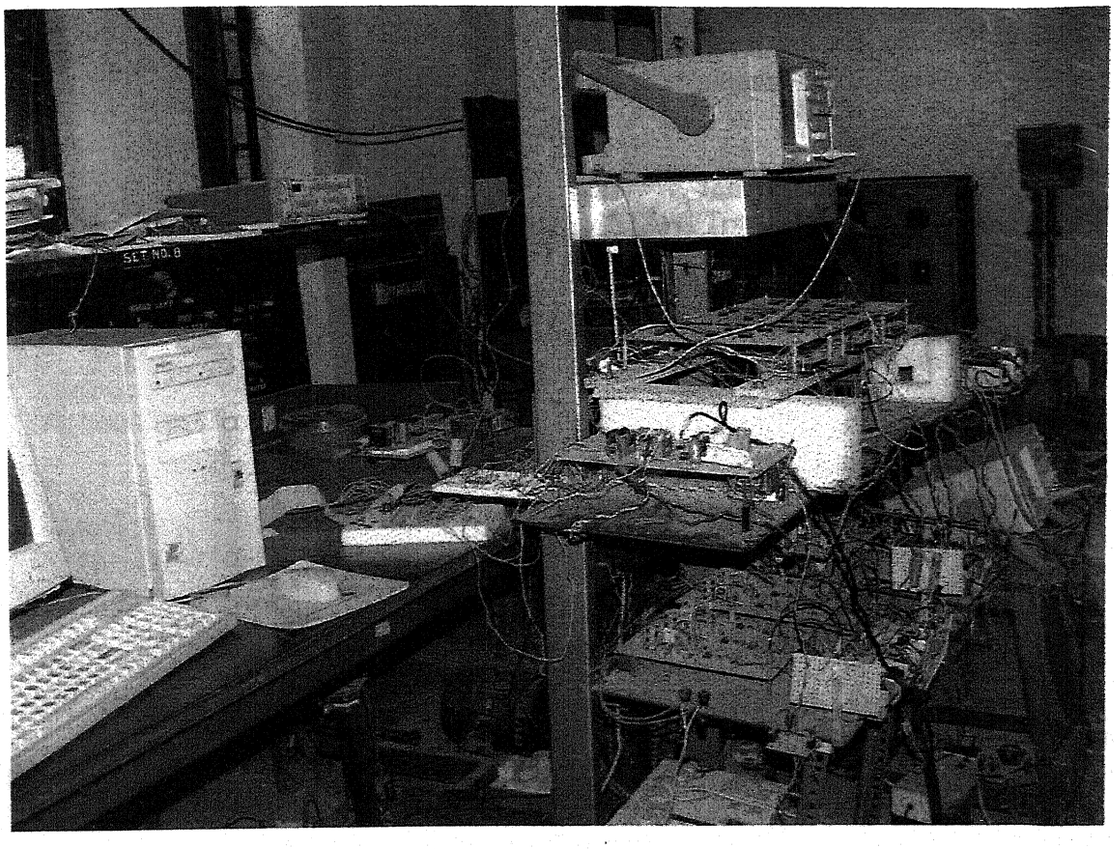
Fig. 5.21. Rotor speed (Nr) and Armature voltage of dc generator (V_{arm}) when load switch is closed at observer gain 'k' = -0.01 and armature current of dc generator = 1 amp,

scheme is analyzed by both SABER simulation and experiment. The soft-switching of inverter devices as the well as independent control of torque and flux have been verified from simulation as well as by experiment. Further, the soft-switching DTC scheme has been extended to include a reduced-order stator flux observer, robust and insensitive to speed variation. From the SABER simulation of the observer-based DTC scheme, it has been found that the stator flux from the observer approaches closely the flux obtained from the mathematical model of the induction machine. The experiment is conducted on a laboratory-sized induction machine both with and without observer. The results obtained from experiment compare well with those obtained from simulation. The observer gain is properly designed and tuned to work satisfactorily with the experimental setup. The comparison between the stator flux obtained from the observer and the flux obtained from the mathematical model of the induction machine reveals implementation of this scheme up to expectation. It is observed that the scheme with the observer provides better performance than the one without the observer.

This detailed study of the QRDCL inverter reveals that the proposed topology can be used for power supplies and high performance induction motor drives as well. Because of soft-switching, and the high performance of the inverter, it can also find application in airborne power supplies.

6.2 Scope for Further Work

1. To undertake detailed losses in ac drives fed from the proposed resonant link inverter.
2. To reduce the number of switches in the proposed topology.
3. To study the possibility of the elimination of switches in series with the dc link while dealing with high power applications. It should be able to work satisfactorily with low power factor loads.
4. To investigate application of QRDCL to UPS and SMPS.



Photograph of the Experimental Setup (Side-view)

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Appendix-A

ACL-8112 PG Enhanced Multi-function Data Acquisition Card

ACL-8112PG is a Enhanced Multi-function Data Acquisition Card which provides the following advanced features.

A.1 Features

- AT-Bus
- 16 single-ended analog input channels.
- Bipolar input signals
- Programmable gain: 5 Levels programmable gain (x1, x2, x4, x8, x16)
- On-chip sample and hold
- Two 12 monolithic multiplying analog output channels
- 16 digital output channels
- 16 digital input channels
- 3 programmable 16-bit down counters
- Programmable sampling rate of up to 100 kHz.
- Three A/D trigger modes: software trigger, programmable pacer trigger, external pulse trigger.
- AT interrupt IRQ capability: 9 IRQ levels (IRQ 3 ~ IRQ 15) are jumper selectable.
- Integral Dc-to-Dc converter for stable analog power source
- 37-pin D-type connector

A.2 Analog Input (A/D Converter)

- Converter : ADS774, successive approximation type
- Input channels : 16 single-ended
- Resolution : 12-bit

- Input Range : Software controlled(Bipolar (±10V, ±5V, ±2.5V, ±1.25V, ±0.625V, ±0.3125V)
- Conversion Time : 8μ sec
- Overvoltage protection: Continuous ±35 V maximum
- Accuracy : 0.015% of FSR ± 1 LSB for gain = 0.5,1,2,4
  : 0.02 % of FSR ± 1 LSB for gain = 8,16
- Input Impedance : 10 MΩ
- Trigger Mode : Software, Pacer, and External trigger
- Data Transfer : Program control, DMA, Interrupt
- Data Throughput : 100 kHz (maximum)

A.3 Analog Output (D/A Converter)

- Output channel : 2 double-buffered analog outputs
- Resolution : 12 –bit
- Output range : Internal reference : (unipolar) 0~5 V or 0~10 V
  : External reference : (unipolar) max. +10V or –10V
- Converte : DAC 7541
- Settling Time : 30 μ sec
- Linearity : ± ½ bitLSB
- Output driving : ± 5 mA max.

A.4 Digital I/O (DIO)

- Channel : 16 TTL compatible inputs and outputs
- Input Voltage : {(Low : Min. 0V, Max. 0.8V), (High : Min. + 2.0 V) }
- Input Load : (Low : + 0.5V @ -0.2 mA max.)
  : (High : +2.7V @ +20mA max .)
- Output Voltage : (Low : Min. 0V; Max. 0.4V)

: (High: Min. +2.4 V)

- Driving Capacity : Low : Max. + 0.5V at 8.0 mA (Sink)
  : High : Min. 2.7V at 0.4 mA (Source)

A.5 Programmable Counter

- Device : 8254
- A/D pacer : 32-bit timer (two 16-bit counter cascaded together) with a 2 MHz time base
- Pacer Output : 0.00046 Hz ~ 0.5 MHz
- Counter : One 16-bit counter with internal 2 MHz time base or external clock source.

Appendix-B

Voltage and Current Sensors

B-1 Voltage Sensor

PCB Mounting Hall Effect Voltage Transducer (Model LV 25-P)

Technical Specifications:

- Nominal current I_N : 10 mA
- Nominal analogue output current : 25 mA
- Turns ratio : 2500:1000
- Supply Voltage : ± 15 V (± 5%)
- Isolation : 2.5 kV (rms)/50 Hz/1 min
- Linearity : < 0.2%
- Response time : < 40 μs for R1 series 25 kΩ resistor
- Operating temperature : 0°C to 70°C
- Current Consumption : 10 mA + output current
- Primary internal resistance : 250 Ω (at 70°C)
- Secondary internal resistance : 110 Ω (at 70°C)
- Weight : 22 g
- Operating range : 10 to 500 V
- Polarity marking : A positive output current is obtained on terminal M when a positive voltage is applied on terminal +HT of the primary circuit.
- Primary resistor R_1 : The transducer's optimum accuracy is obtained with the nominal primary current. As for as possible, R1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10mA.
- Measuring resistance with ± 15 V at ± 10 mA max. R_M min. 100 Ω; R_M max. 350 Ω

at ± 14 mA max.	100 Ω	190 Ω

Connection pins

Pin + : Supply voltage +15 V

Pin M : Measuring point

Pin - : Supply voltage -15 V

Pin + HT : Primary voltage +

Pin - HT : Primary voltage -

B-2 Current Sensor (LEM Module LA 55-P)

This hall effect current transducer can be used for electronic measurement of currents: DC, AC, IMPL., etc., with galvanic isolation between the primary (high power) and the secondary (electronic) circuits.

Electrical Data

Nominal current IN : 50 A

Measuring Range : 0 to ± 70 A at 70°C

Measuring resistance :		at + 70°C		at + 85°C	
		R_M min.	R_M max.	R_M min	R_M max.
With ± 12 V	at ± 50 A max.	10 Ω	100 Ω	60 Ω	95 Ω
	at ± 70 A max.	10 Ω	50 Ω	60 Ω	60 Ω
With ± 15 V	at ± 50 A max.	50 Ω	160 Ω	135 Ω	155 Ω
	at ± 70 A max.	50 Ω	90 Ω	135 Ω	135 Ω

Nominal analog output current : 50 mA

Turns ratio : 1:1000

Accuracy at +25°C and at ± 15 V (± 5 %) : ±0.65 % of I_N

Accuracy at +25°C and at ± 12 V to ± 15 V : ±0.9 % of I_N

Supply voltage : + and - 12 to 15 V (± 5 %)

Isolation between primary and secondary : 2 kV rms/50 Hz/1 min.

Accuracy-Dynamic performance

Zero offset current at ± 25°C	: max. ± 0.2 mA	
Residual current after an overload of 3x I_N	: max. ± 0.3 mA	
Thermal drift of offset current		
(between 0°C and +70°C)	: typical ± 0.1 mA	max. ± 0.5 mA
(between -25°C and +85°C)	: typical ± 0.1 mA	max. ± 0.6 mA
Linearity	: better than 0.15%	
Response time	: inferior at 500 nS	
Rise time	: better than 1 μs	
di/dt accuracy followed	: better than 200 A/μs	
Band width	: 0 to 200 kHz (-1dB)	

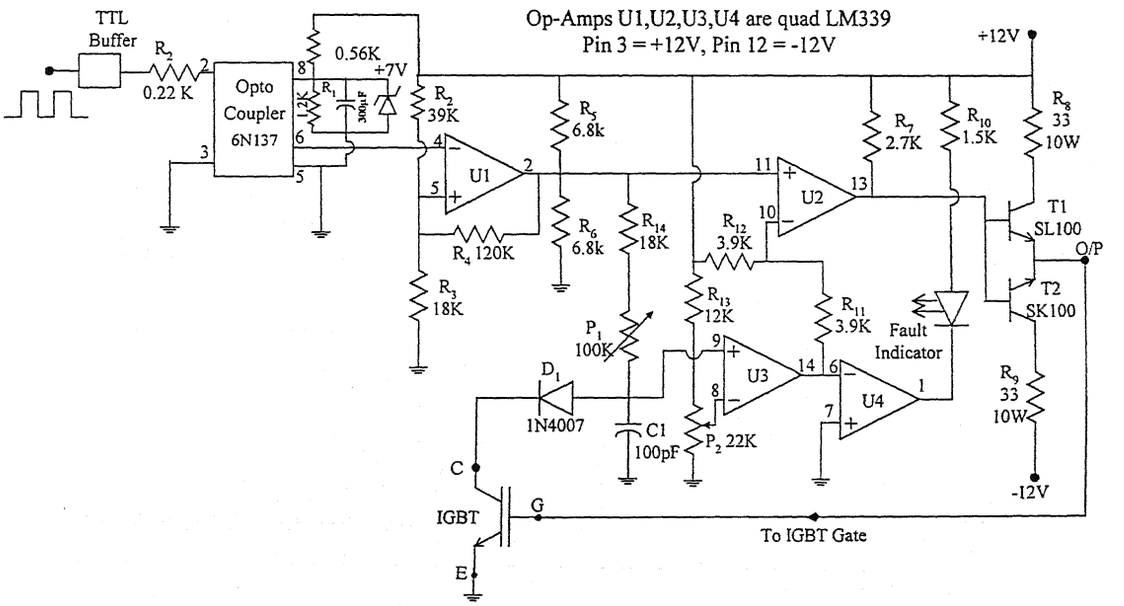
General Data

Operating temperature	: -25°C to +85°C
Storage temperature	: -40°C to +90°C
Current consumption	: 10 mA (at ± 15 V) + output current
Secondary internal resistance	: 80 Ω (at +70°C), 85 Ω (at +85°C)
Weight	: 18 g

Appendix-C

Driver Circuit of IGBT, Opto-Isolator (6N137), Specification of IGBT and Induction Motor parameters

C.1. DRIVER CIRCUIT OF IGBT:



C.2. OPTO-ISOLATOR (6N137)

Features

- Super high speed response (t_{PLH} , t_{PHL}: 45 ns at R_L = 3500 Ω)
- Isolation voltage between input and output (V_{iso}: 2.5 kV rms)
- LSTTL and TTL compatible output
- Instantaneous common mode rejection voltage (Typ 500 V/μs)

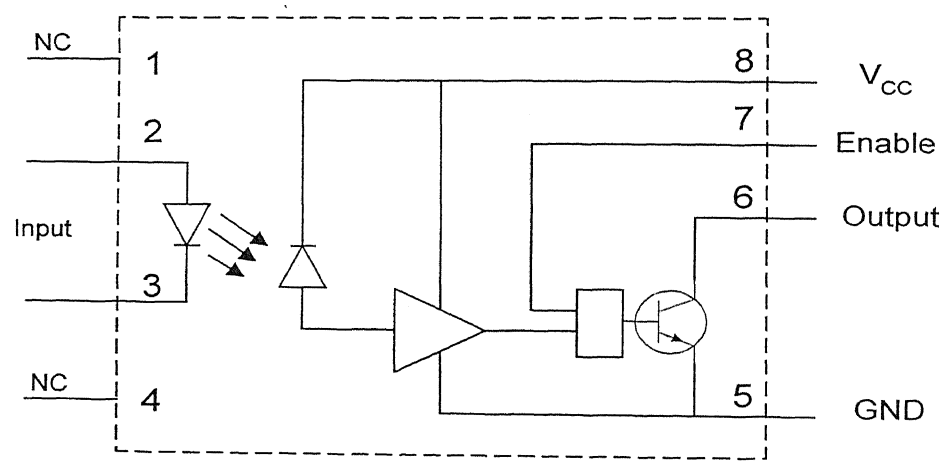
Applications

- High speed interfaces for computer peripherals, microcomputer systems
- High speed line receivers
- Noise reduction
- Interfaces for data transmission equipment

Absolute Maximum Ratings

- Input peak forward current (I_{FM} = 40 mA)
- Input reverse voltage (V_R = 5 V)
- Supply voltage (V_{CC} = 7 V)
- Enable voltage (V_E = 5.5 V)
- Output voltage (V_O = 7V)
- Output current (I_O = 50 mA)
- Operating temperature (T_{OP} = 0 to + 70^0 C)

Pin connection of Opto-Isolator



NC :- No Connection

Fig. C-2: Pin connection of opto-isolator (6N137)

Truth Table		
Input	**Enable**	**Output**
H	H	L
L	H	H
H	L	H
L	L	H

C.3. SPECIFICATION OF DUAL IGBT POWER MODULE

Make : Fuji Electric

Type : 2MB150N-120

Max. Collector-Emitter Voltage (V_{CEM}) : 1200 V

Max. Collector-Emitter Saturated Voltage (V_{CESM}) : 3.3 V

Max. Gate-Emitter Voltage (V_{GEM}) : ± 20 V

Gate-Emitter Threshold Voltage ($V_{GE(th)}$) : 4.5 V

Peak Collector Current (I_{CM}) : 100 A

Collector Current (I_C) : 50 A

(t_{on} = 1.2 μs, t_r = 0.6 μs, t_{off} = 1.5 μs, t_f = 0.5 μs, t_{rr} = 350 ns)

C.4. INDUCTION MOTOR PARAMETERS

Line-to-line : 400 V, Iph (rated) = 2.6 Amp

Stator resistance per phase (R_s)= 8.4 Ω.

Rotor resistance per phase (R_r)= 4.1 Ω.

Stator leakage inductance per phase (l_s) = 0.026 H

Rotor leakage inductance per phase (l_r) = 0.026 H.

Magnetizing inductance per phase (L_m)= 0.377 H,

Moment of inertia (J) = 0.02 Kg-m^2

Appendix-D

Flow-Chart of QRDCL Inverter Topology for Low and High pf Load

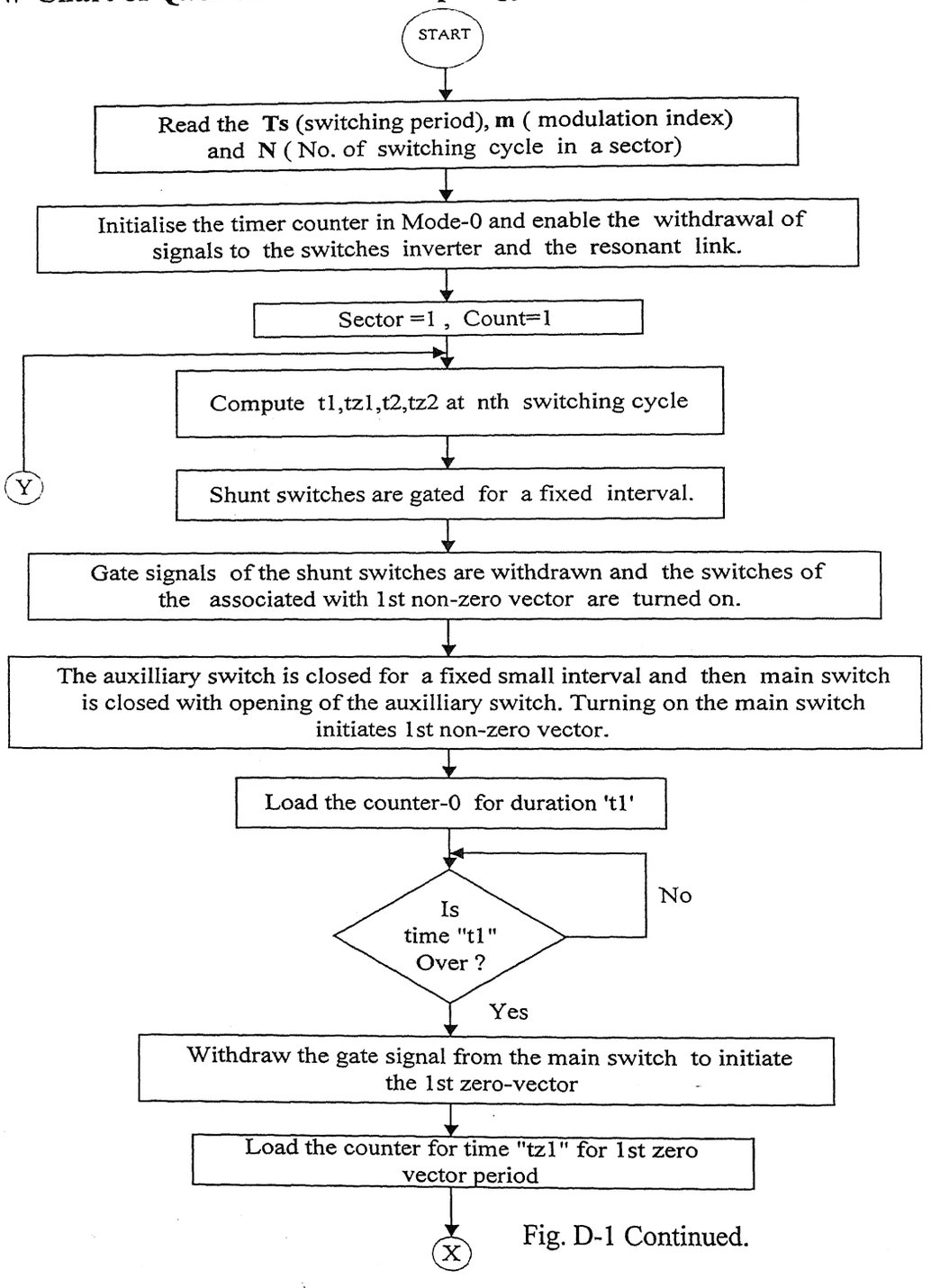


Fig. D-1 Continued.

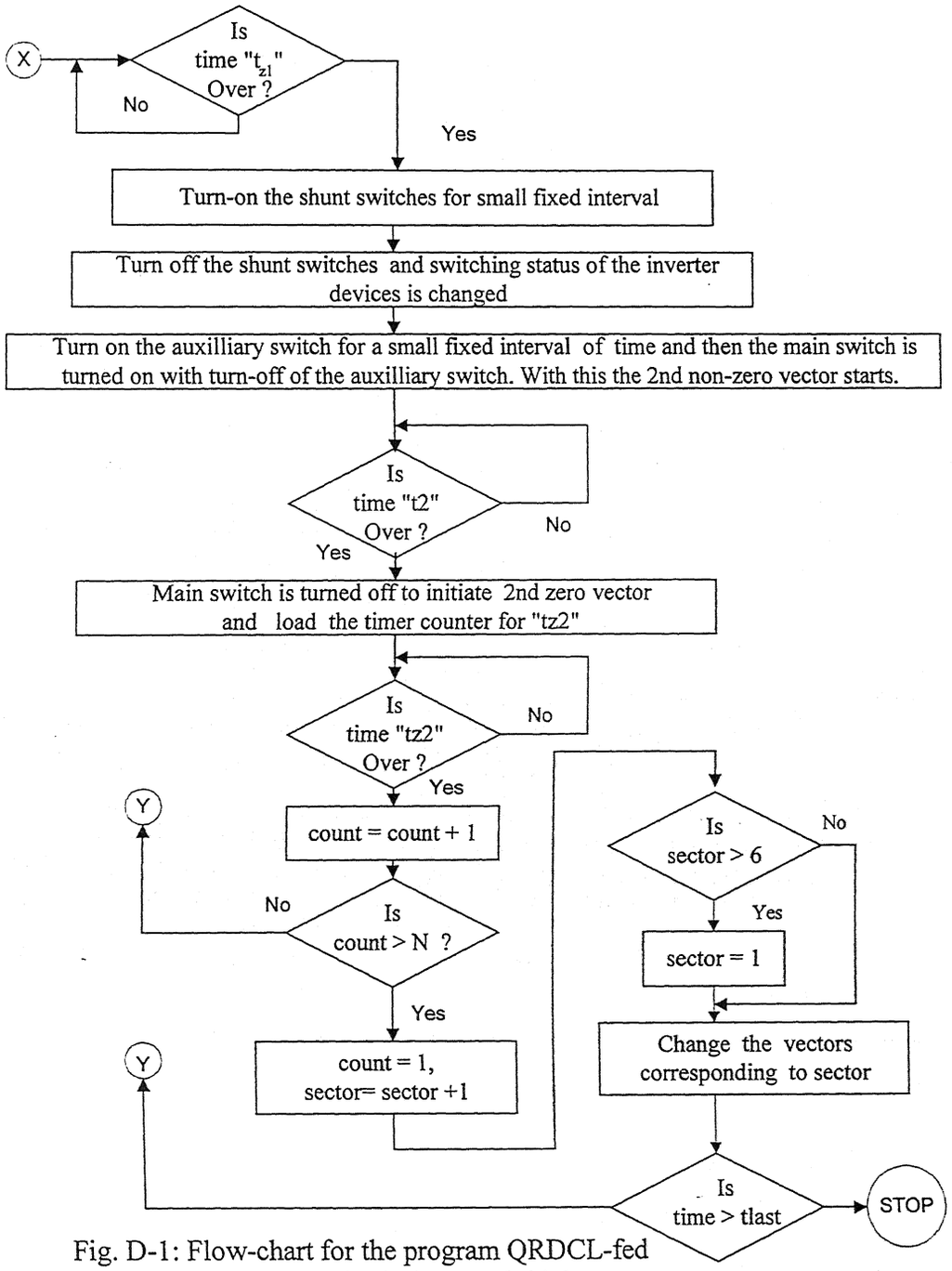


Fig. D-1: Flow-chart for the program QRDCL-fed Inverter operating at both low and high power factor load

Appendix-E

Flow-Chart of QRDCL Inverter-fed DTC

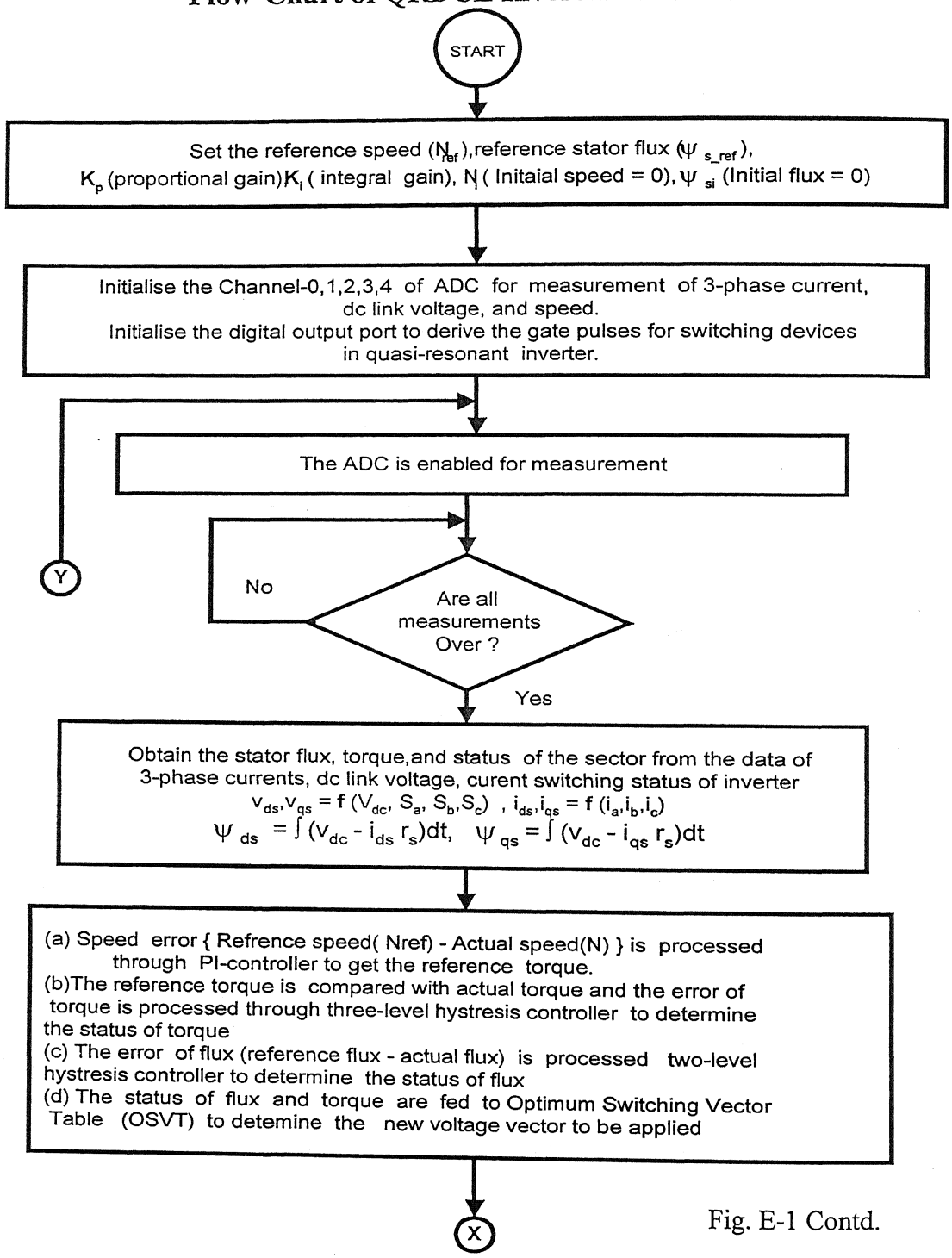


Fig. E-1 Contd.

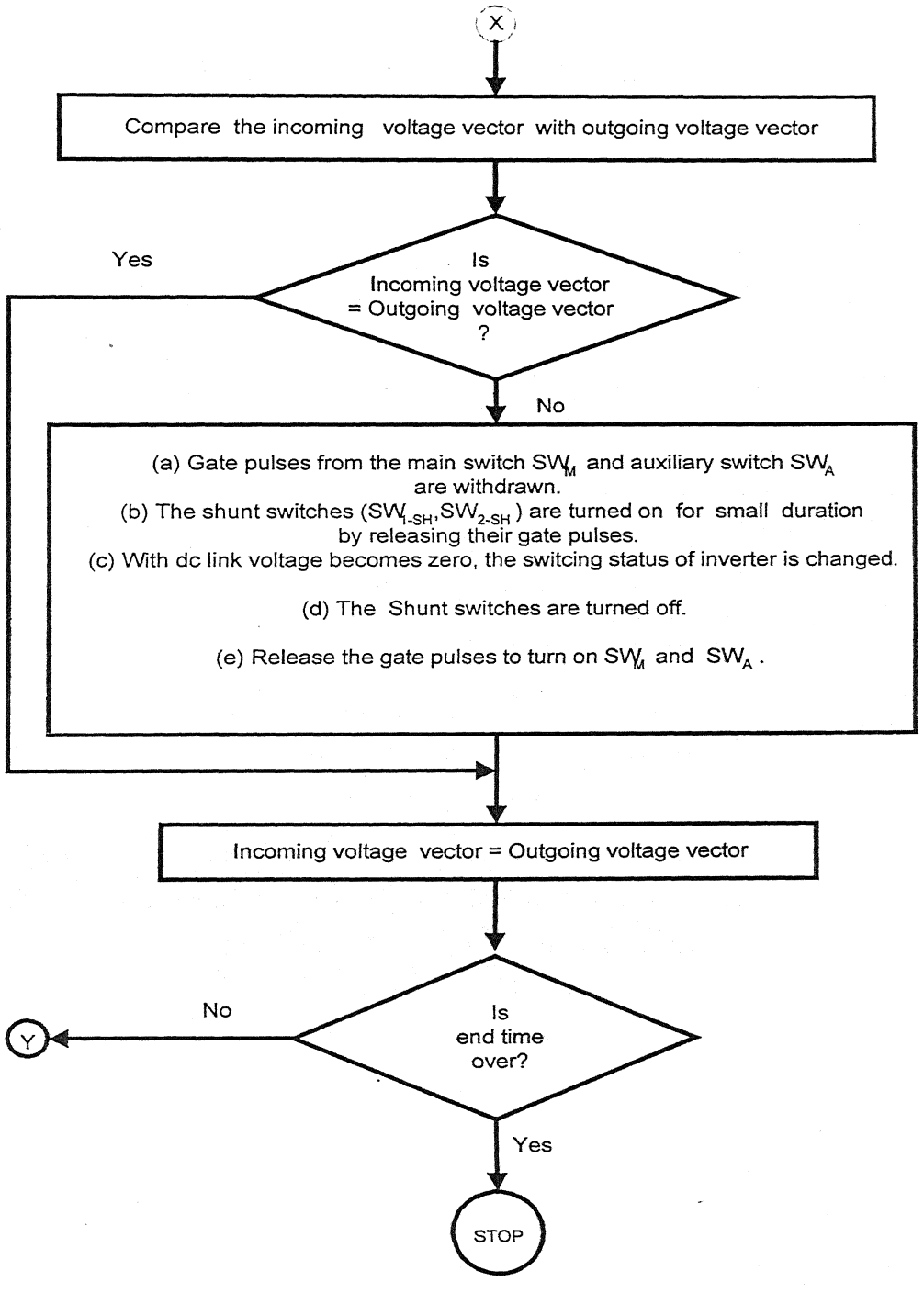


Fig. E-1: Flow-chart for implementing the quasi-resonant inverter-fed DTC scheme (without observer)

Appendix-F

Flow-Chart of QRDCL Inverter-fed DTC with Observer

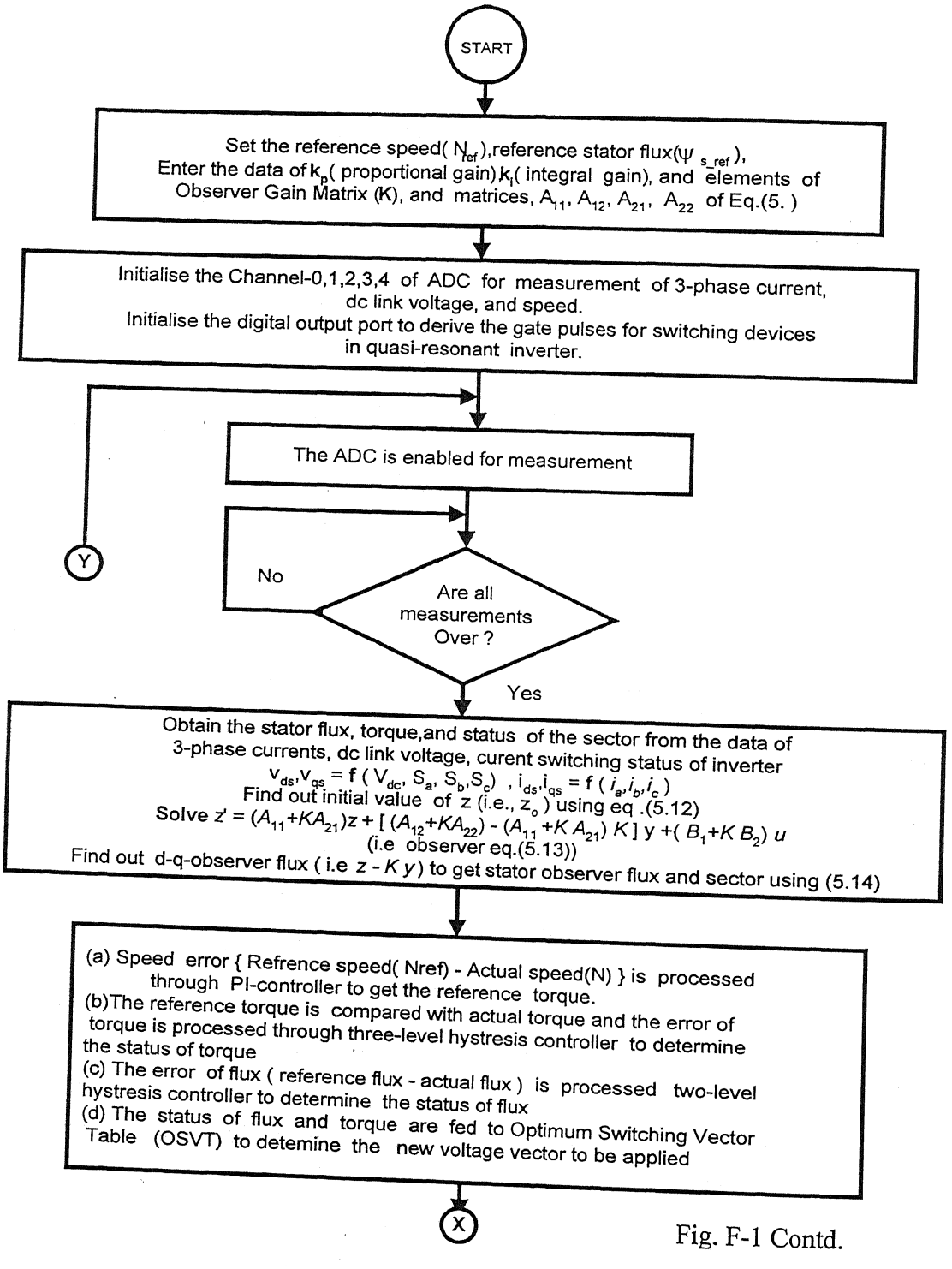


Fig. F-1 Contd.

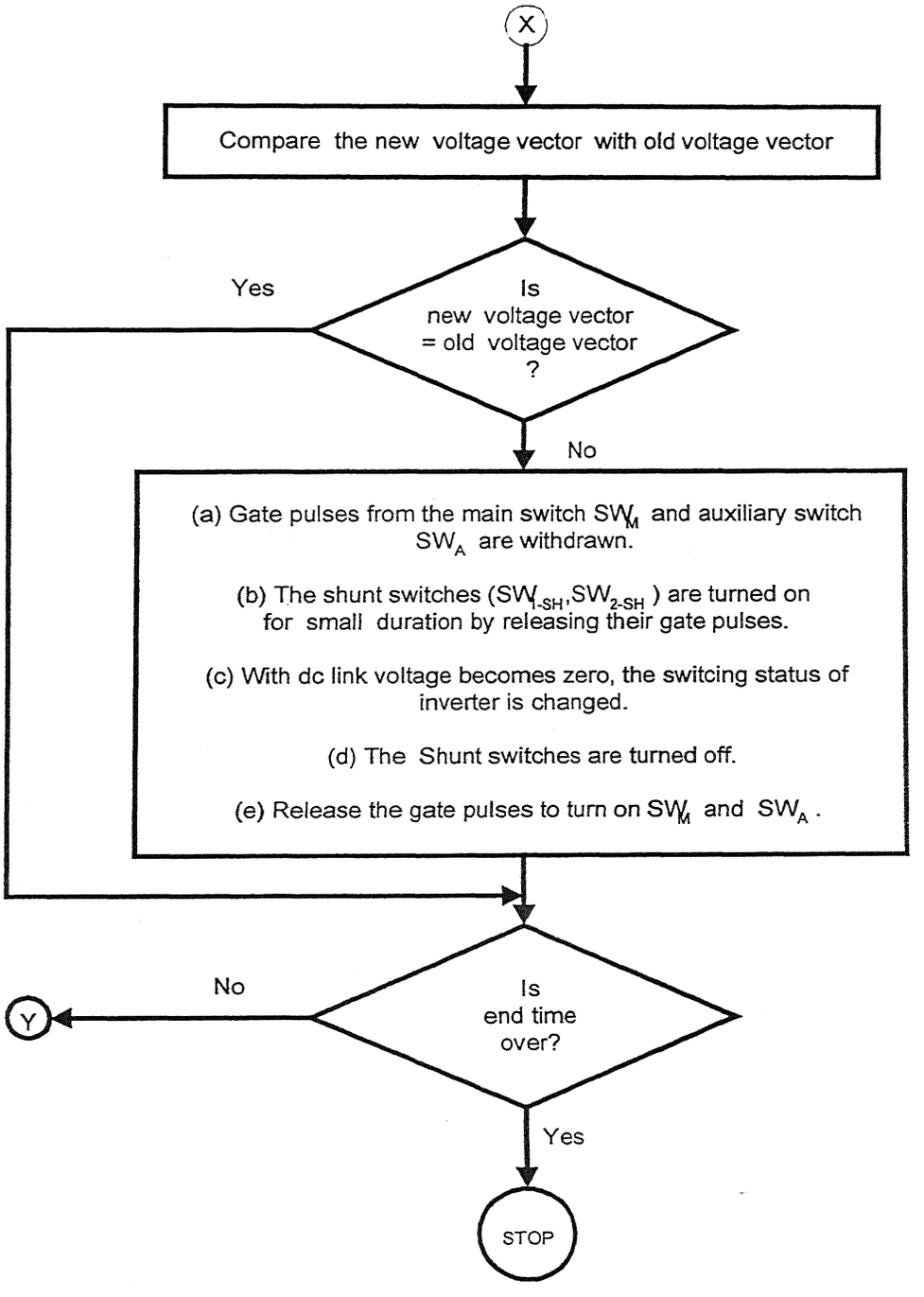


Fig. F-1: Flow-chart for implementing quasi-resonant inverter-fed DTC scheme with **observer**

About the Author

Sribatsa Behera was born in Kendrapara, Orissa, on June 06, 1965. He received the B.Sc. Engg (Electrical) and the M.Tech. (Machine Drives and Power Electronics) degrees from U.C.E. Burla, Sambalpur University, Orissa, India, and Indian Institute of Technology, Kharagpur, India, in 1988 and 1991 respectively. In July 1992 he joined as a Lecturer at U.C.E. Burla, Sambalpur, India. Between 1991-1992, he was working for a brief period in IIT New Delhi and JMI University, New Delhi.

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